

**IN THE DRAWINGS**

The attached sheets of drawings include changes to Figures 1.2A, 1.2B, 1.2C, 1.4, 1.5A, 1.5B, 1.6A and 1.6B. The revisions delete reference numerals not mentioned in the written description. Additionally, in Figure 1.2A, reference numeral "110" and a dashed box have been added to conform Figures 1.1 and 1.2A, and the associated written description. In Figures 1.5A and 1.5B, the title has been deleted. The legend "Prior Art" has been added to Figures 1.2C and 1.4.

The Applicants also note that formal drawings, numbered sheets 1/24- 24/24 have been provided to replace the informal drawings.

**Attachment:** Replacement Sheets 1/24-24/24

Annotated Sheets Showing Changes

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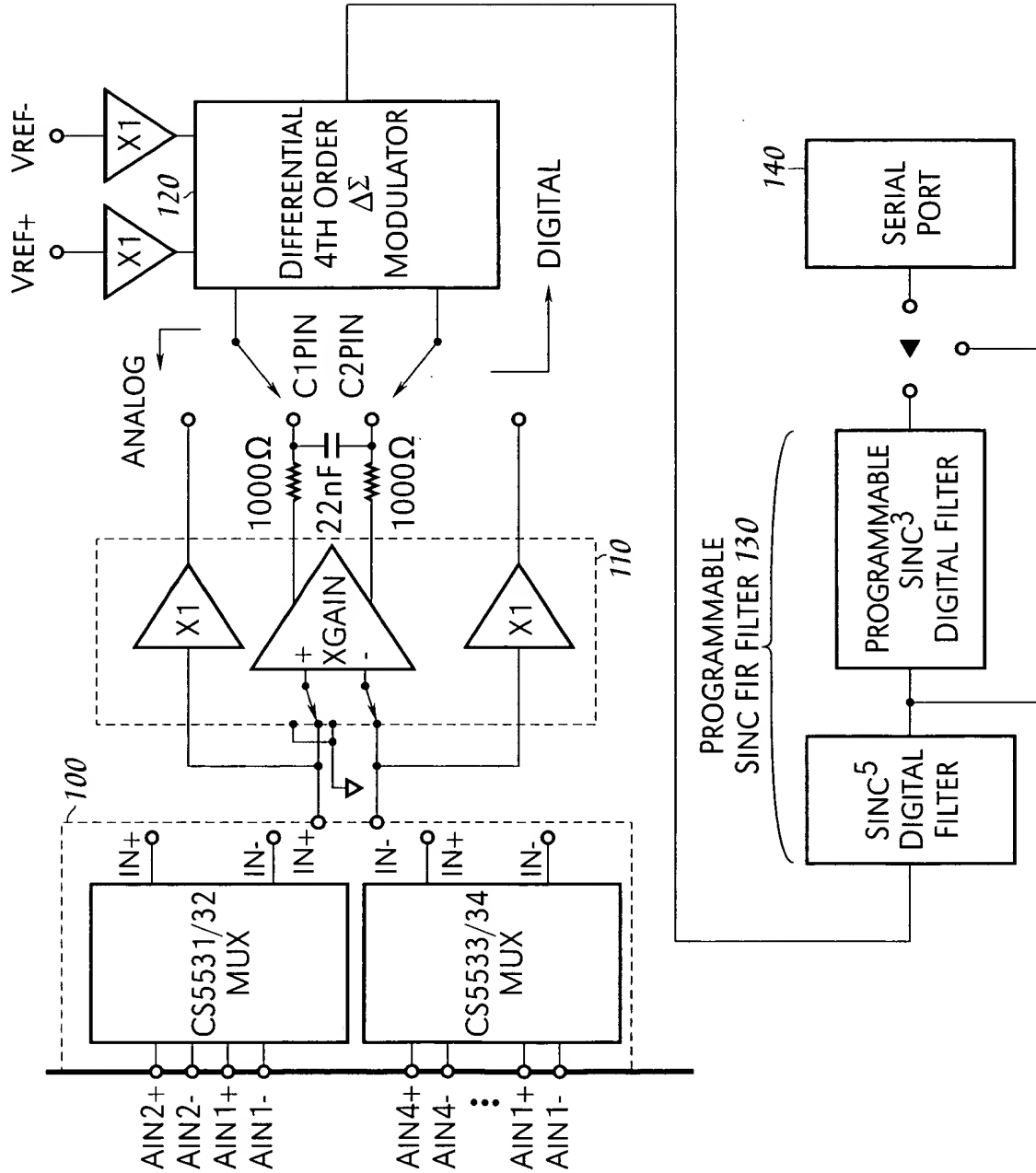


Fig. 1.2A

GAIN IS THE GAIN SETTING OF THE PGIA (I.E. 2, 4, 8, 16, 32)

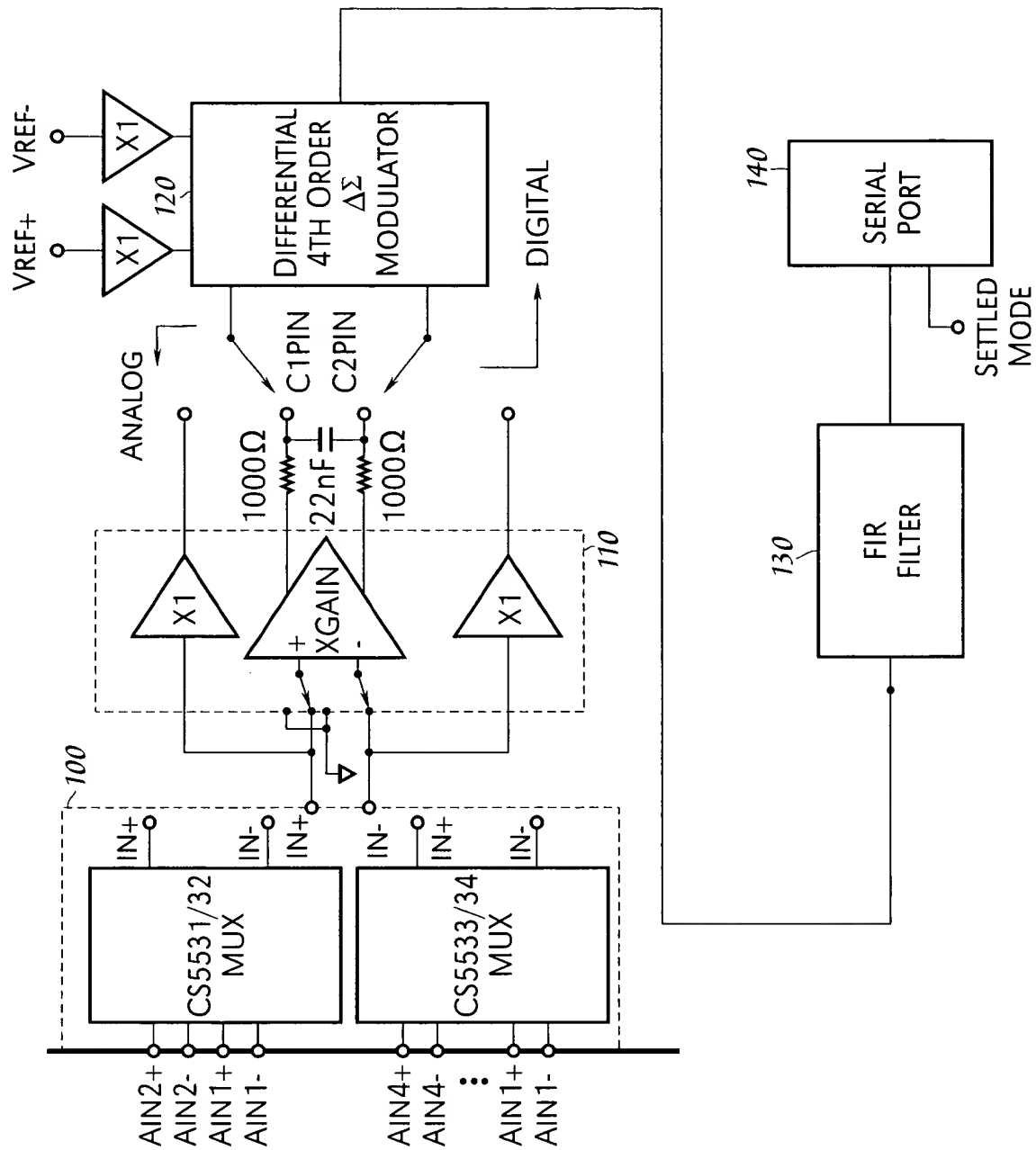


Fig. 1.2B

GAIN IS THE GAIN SETTING OF THE PGIA (I.E. 2, 4, 8, 16, 32)

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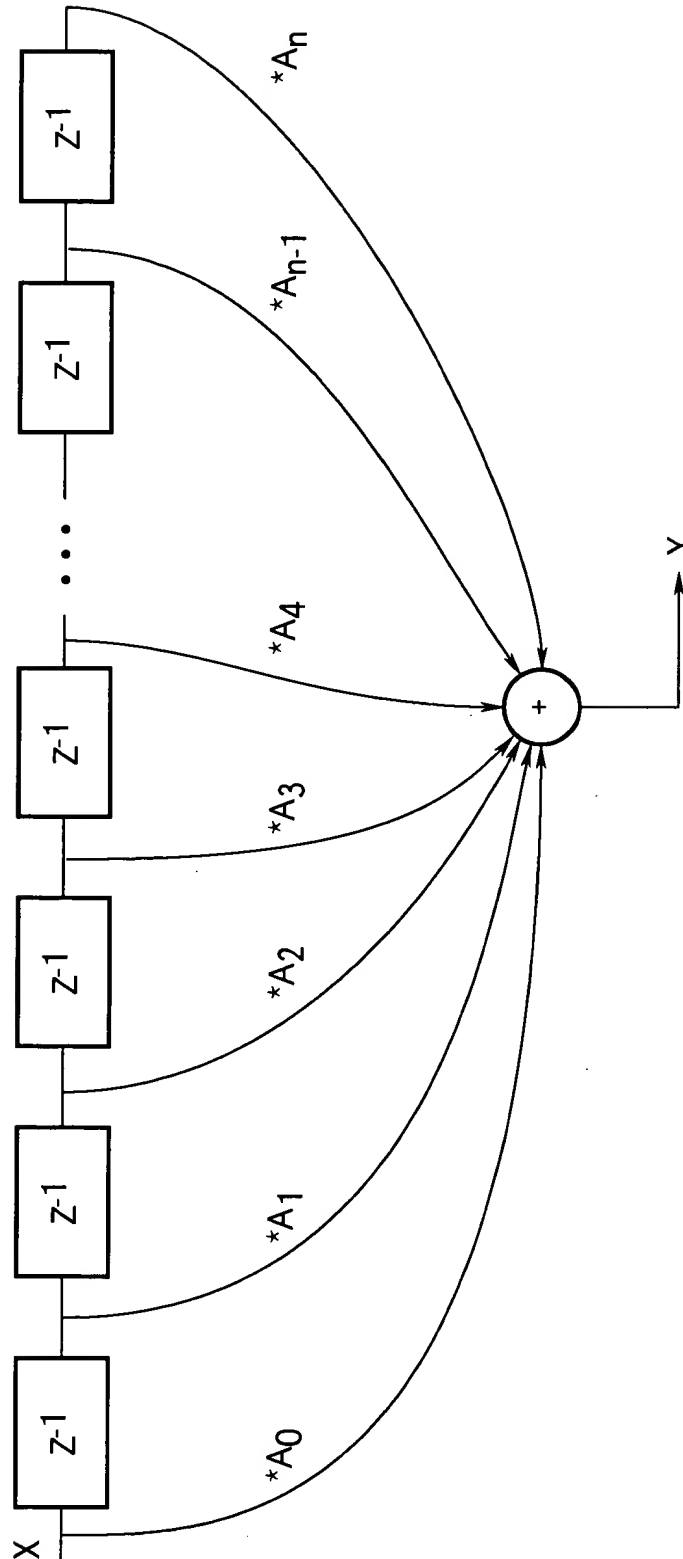


Fig. 1.2C  
(Prior Art)

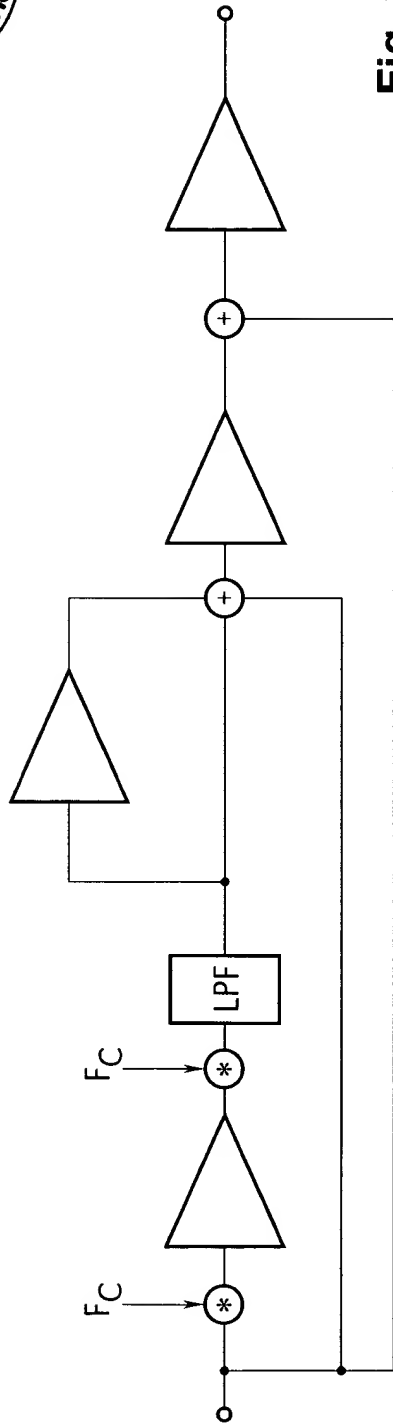


Fig. 1.3

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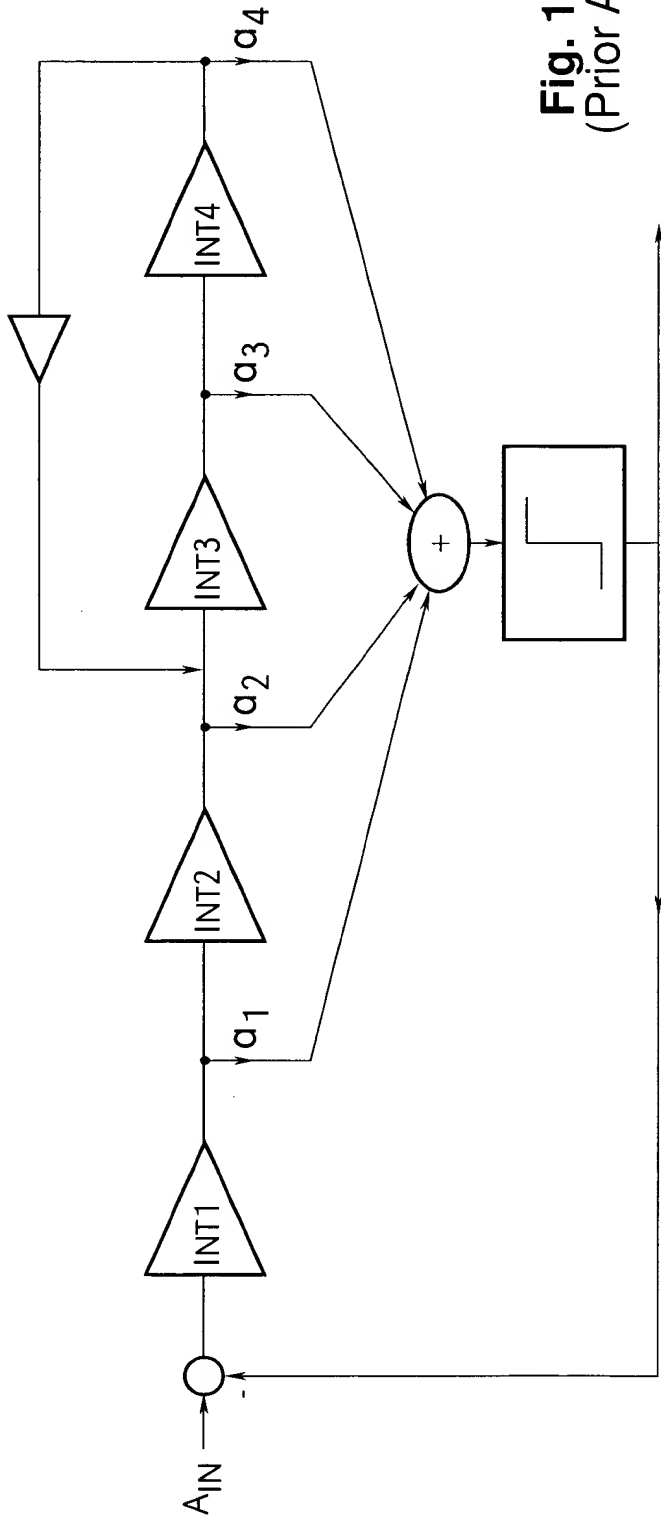


Fig. 1.4  
(Prior Art)

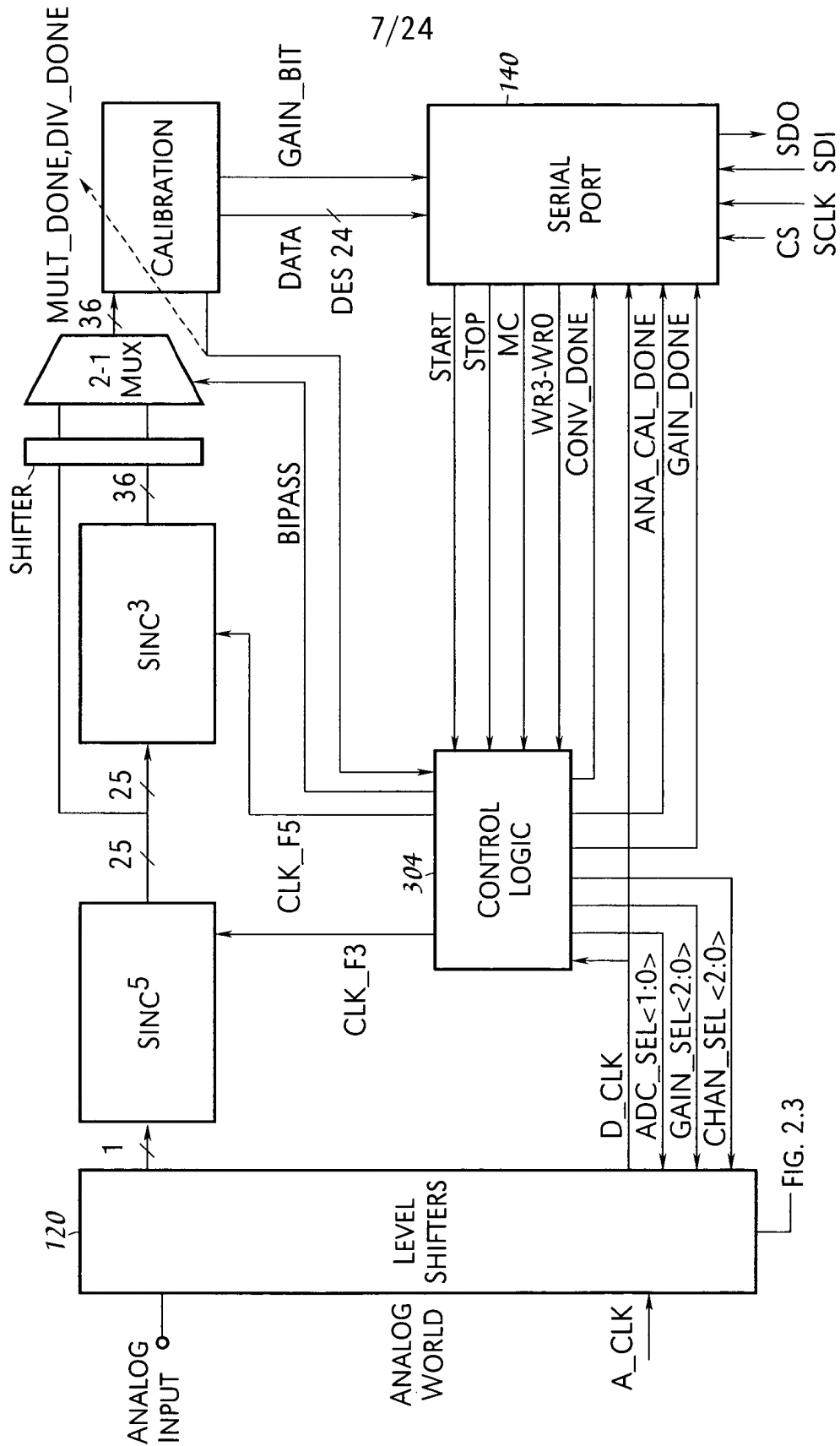


Fig. 1.5A

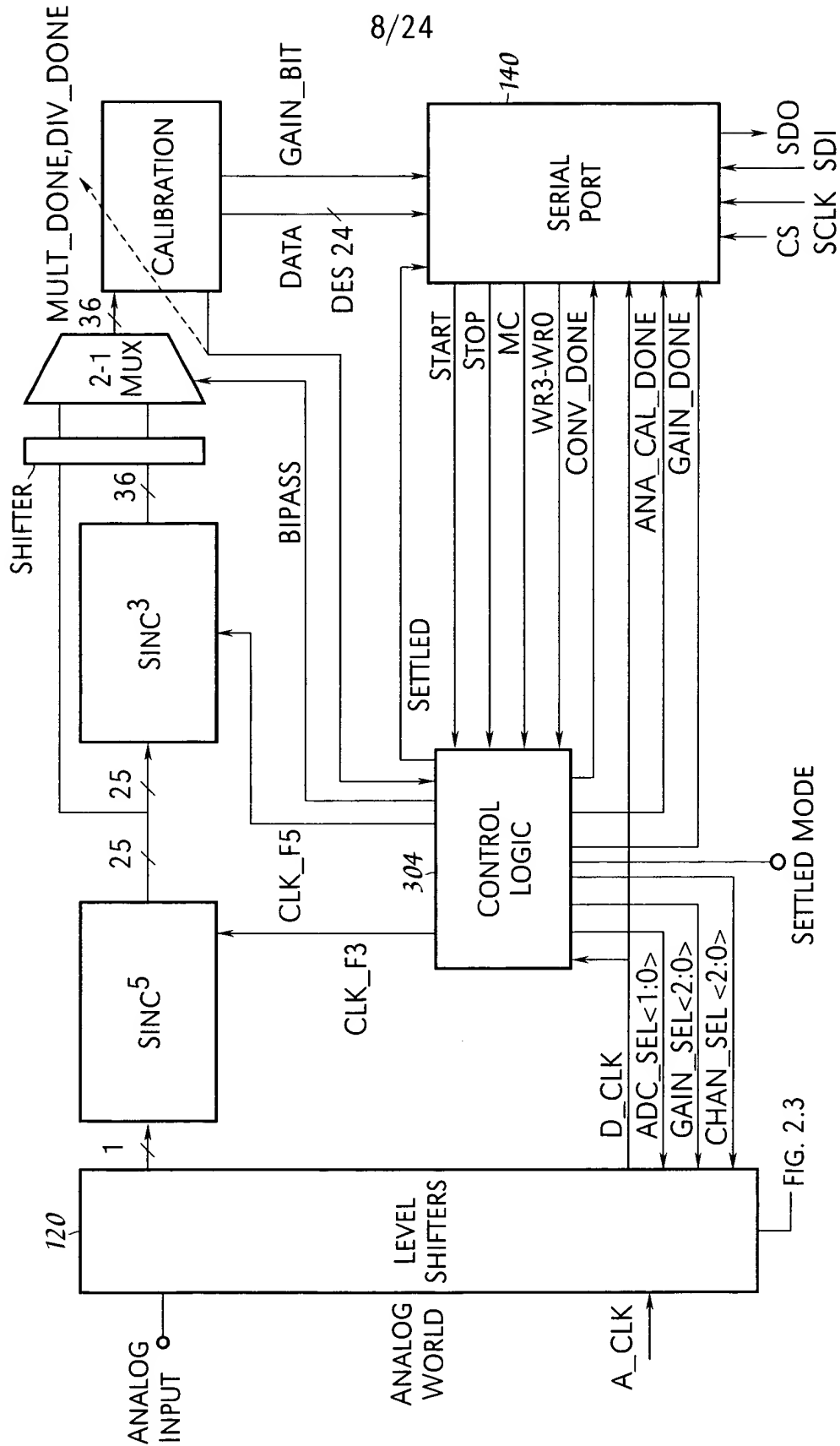
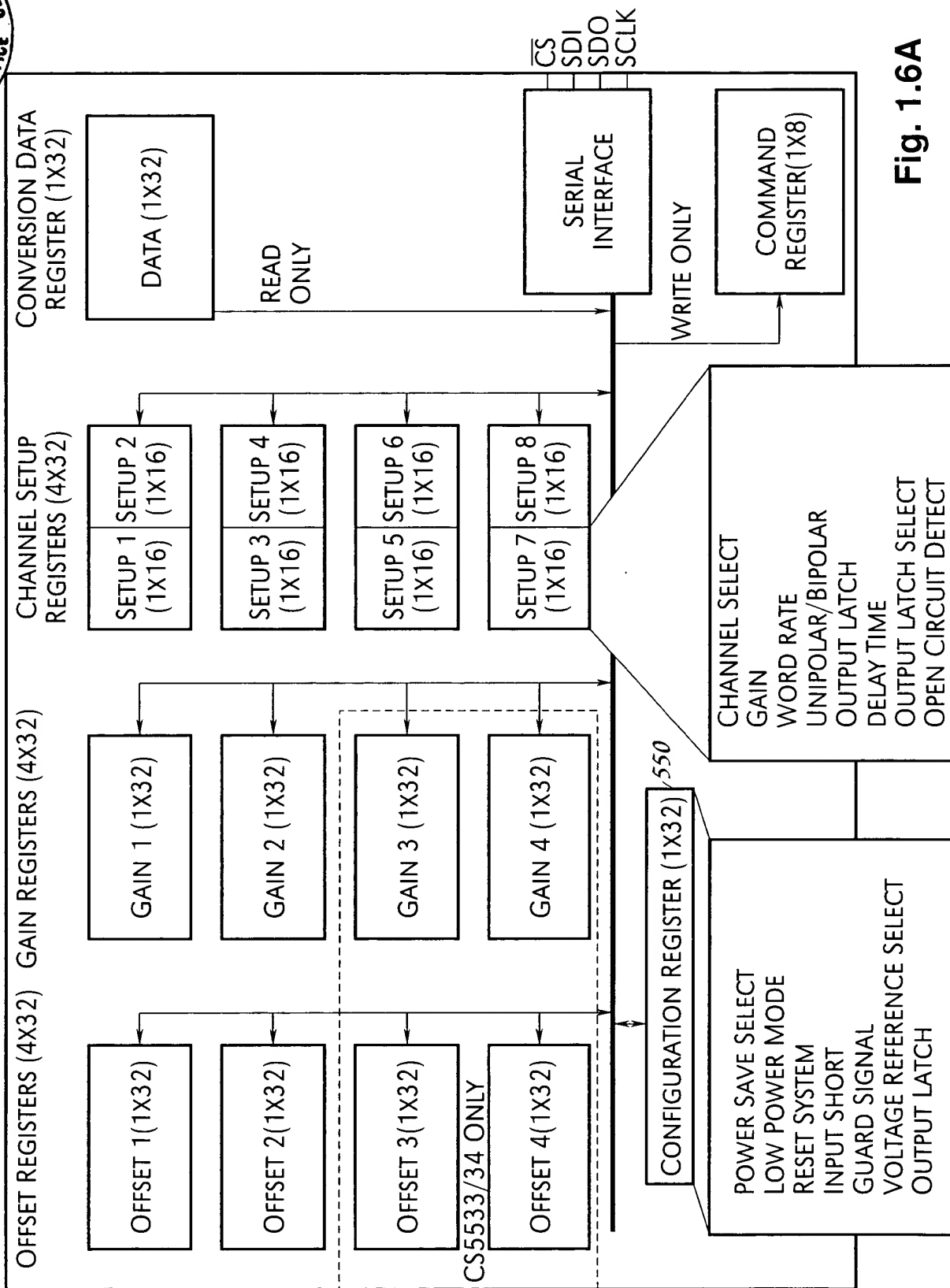


Fig. 1.5B

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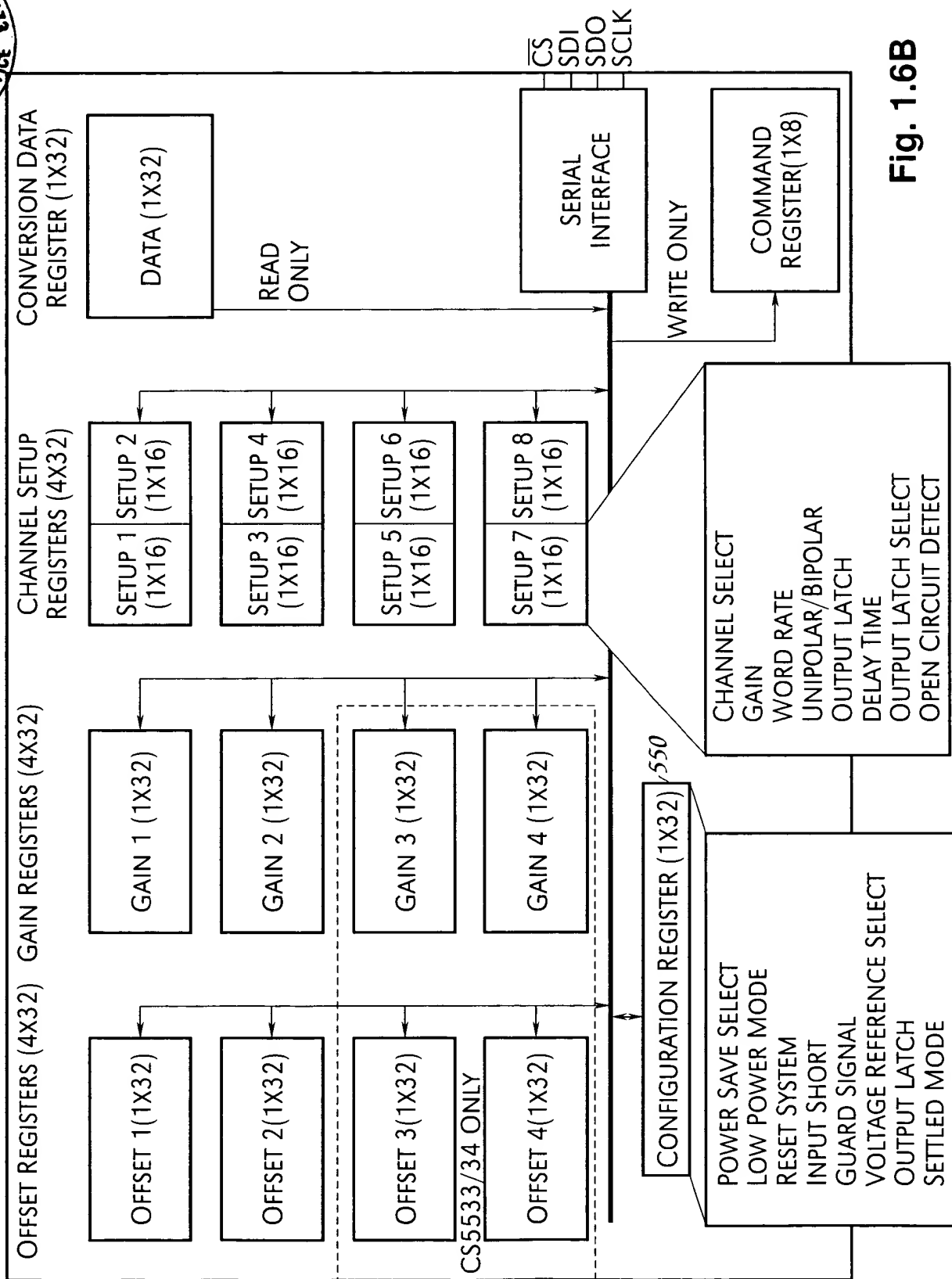


Fig. 1.6B

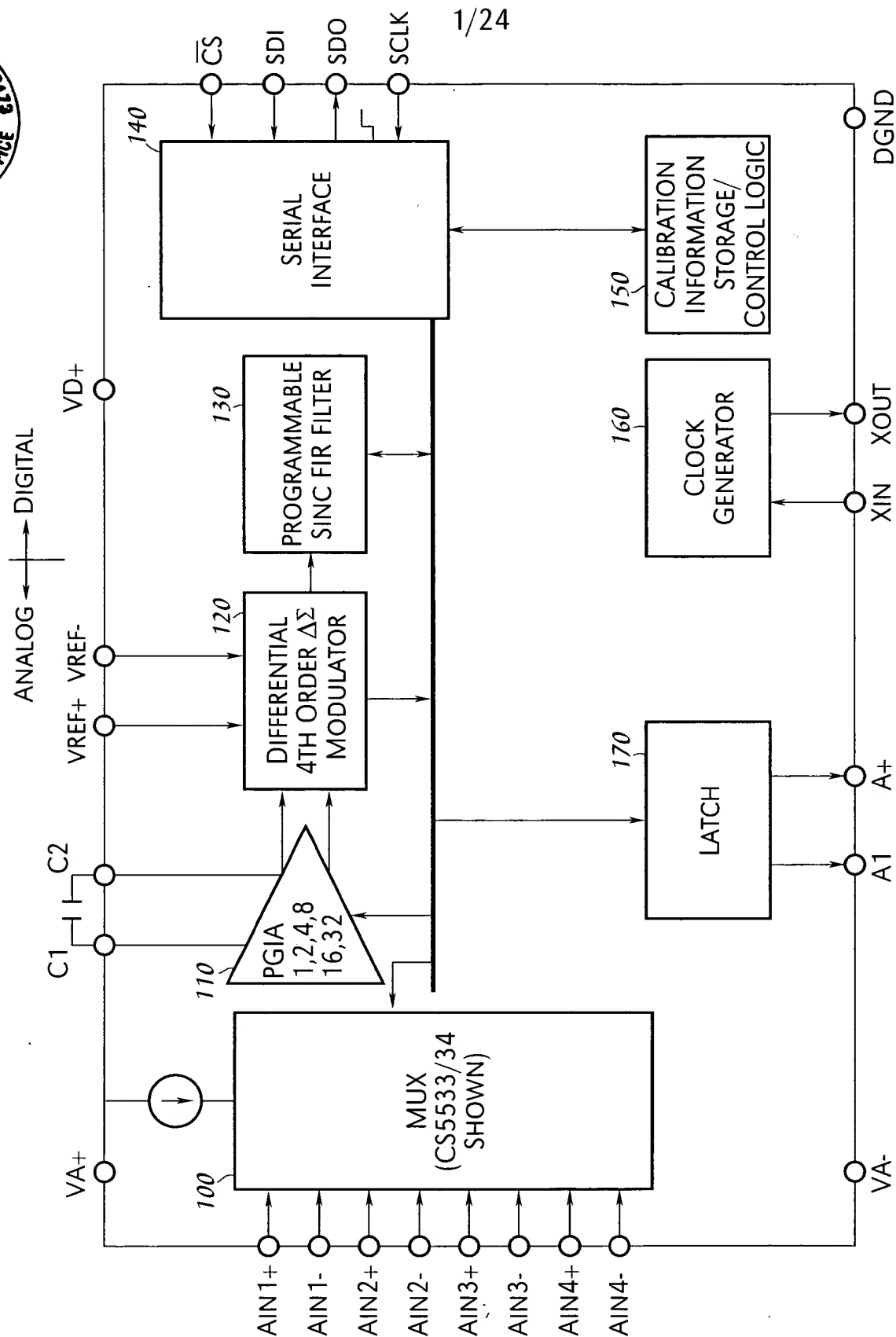


Fig. 1.1A

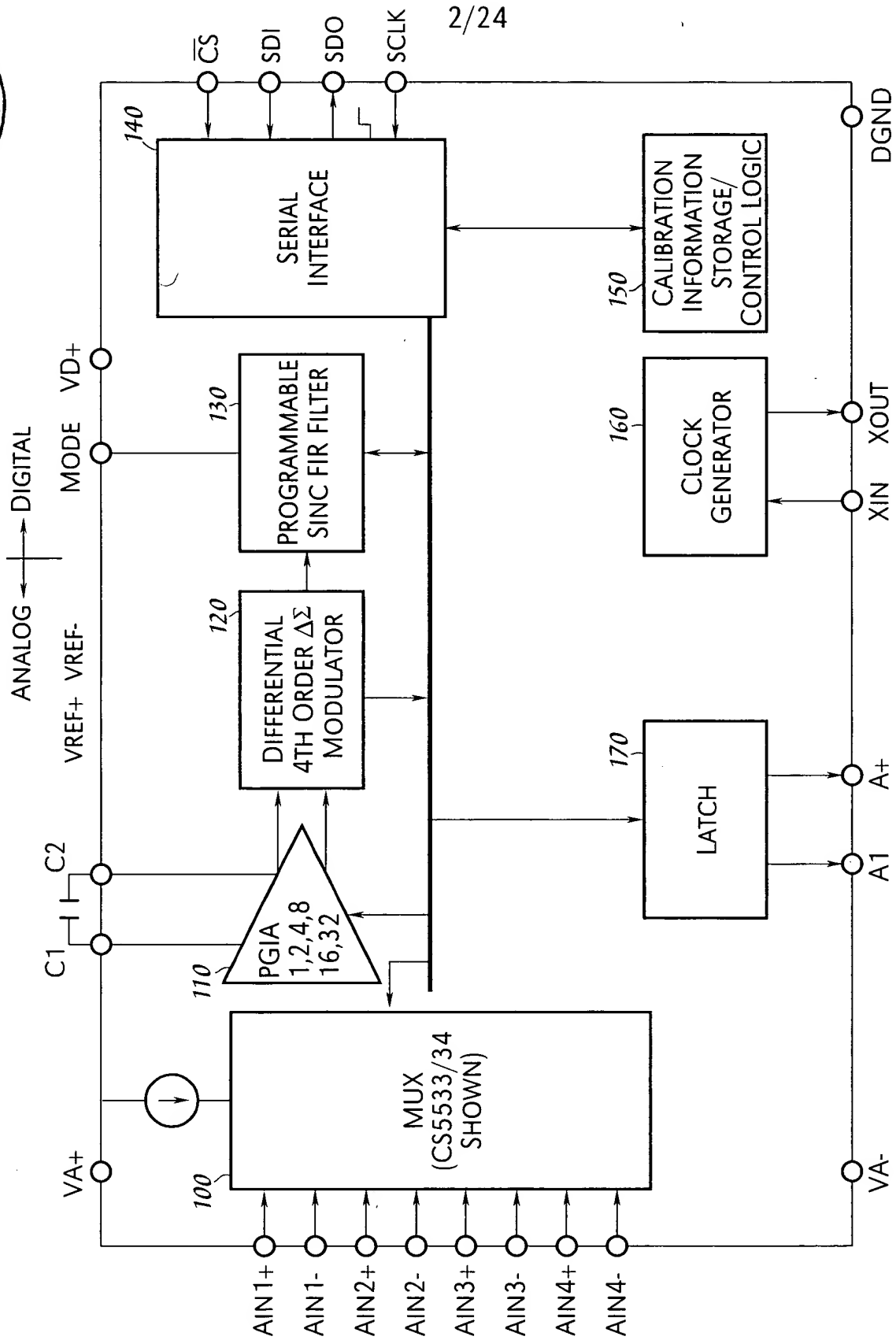


Fig. 1.1B



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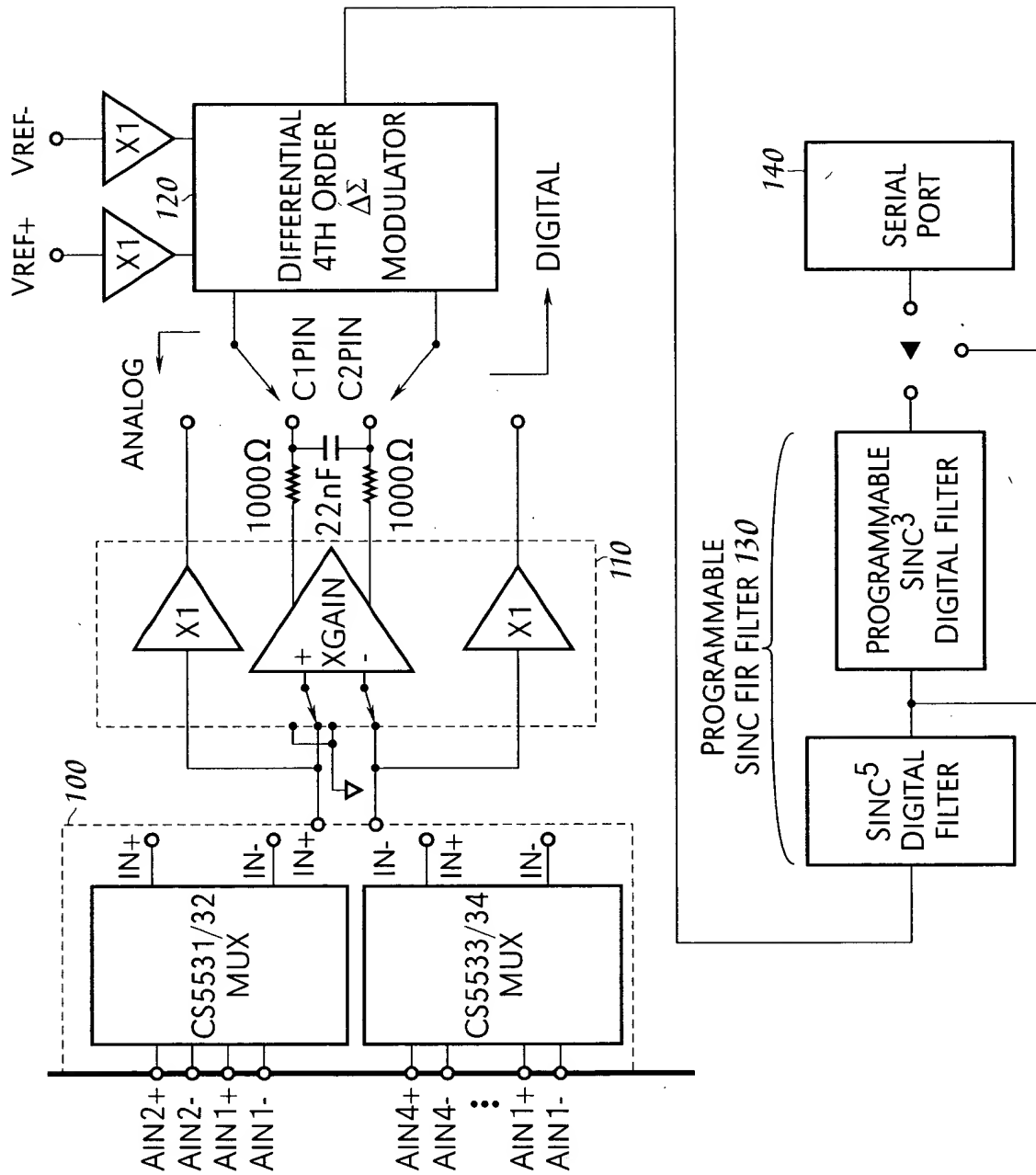


Fig. 1.2A

GAIN IS THE GAIN SETTING OF THE PGIA (I.E. 2, 4, 8, 16, 32)

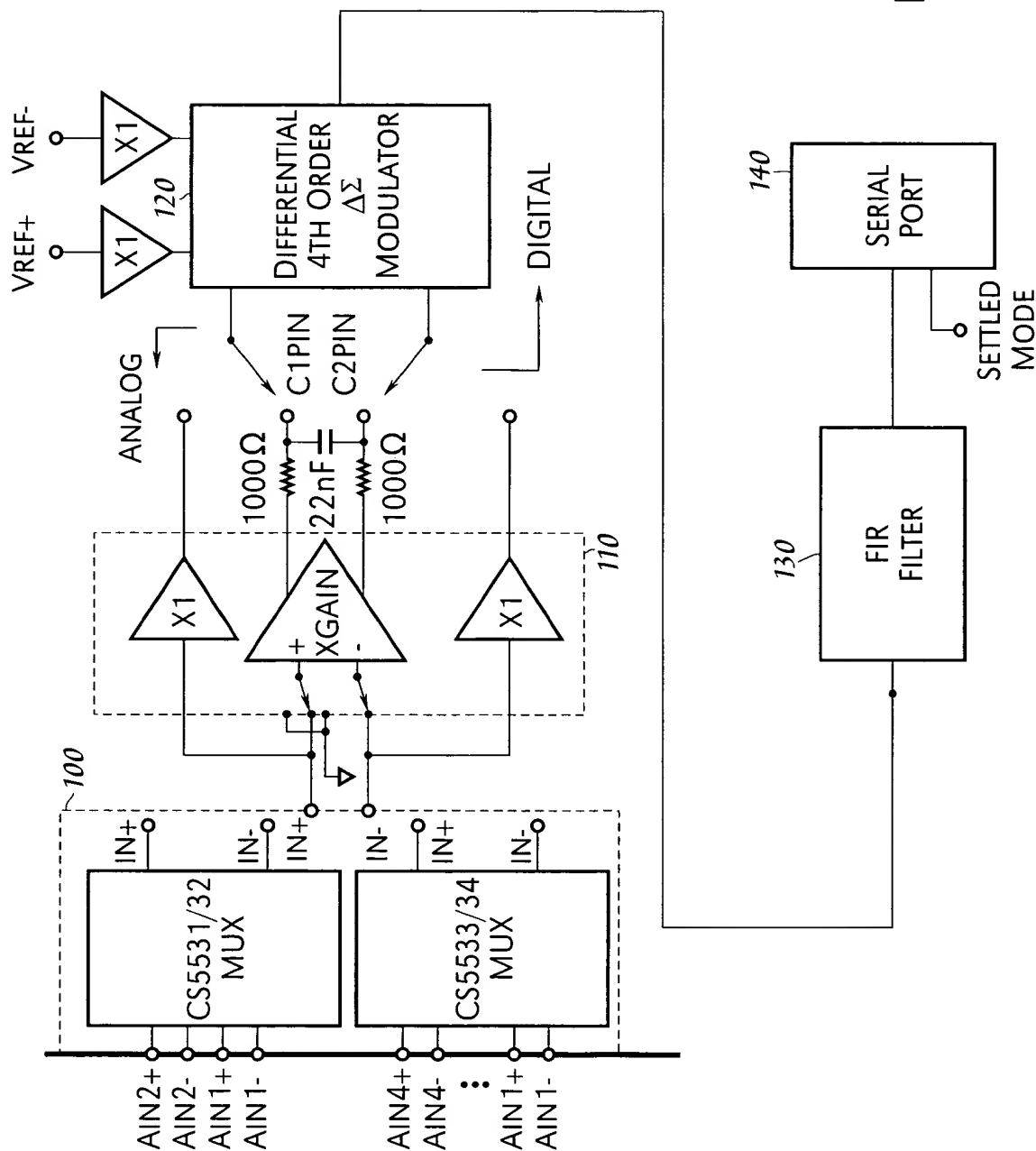


Fig. 1.2B

GAIN IS THE GAIN SETTING OF THE PGIA (I.E. 2, 4, 8, 16, 32)



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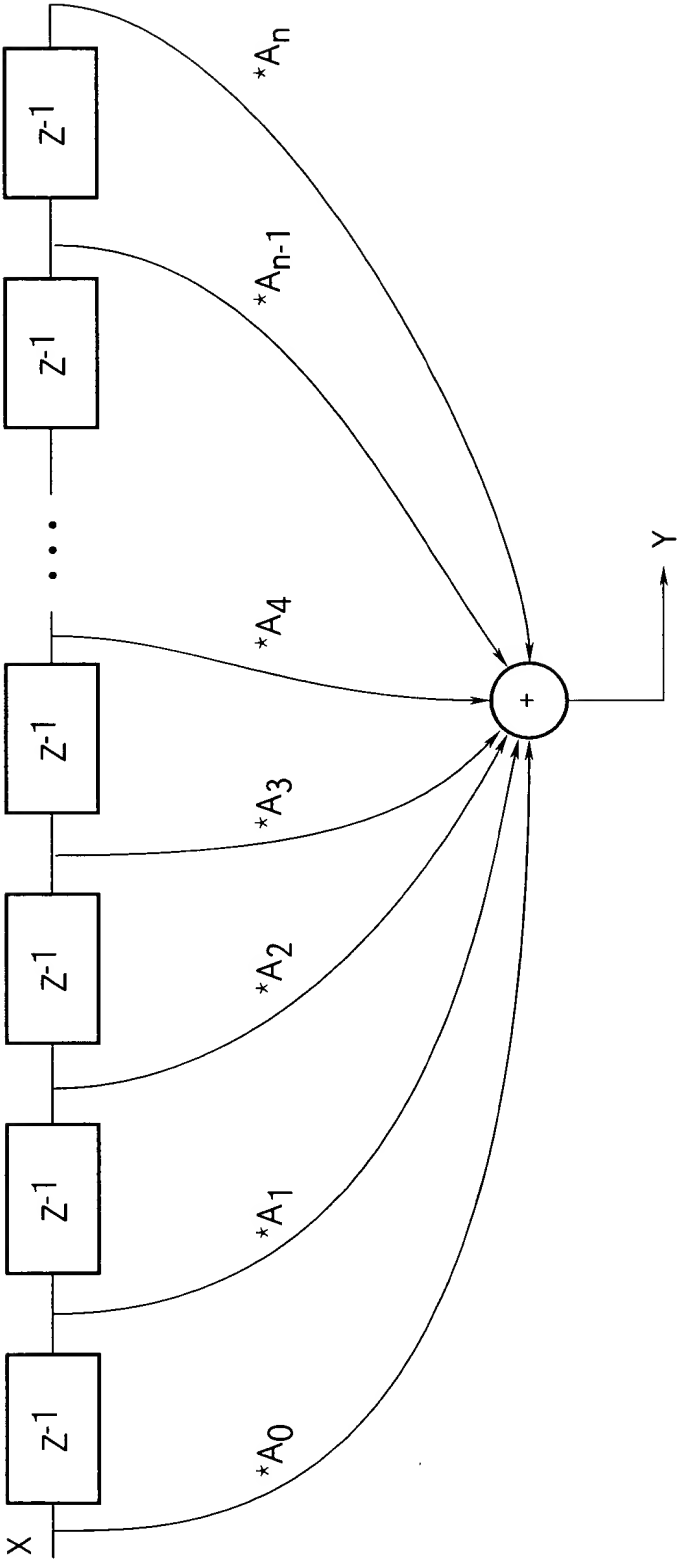


Fig. 1.2C  
(Prior Art)

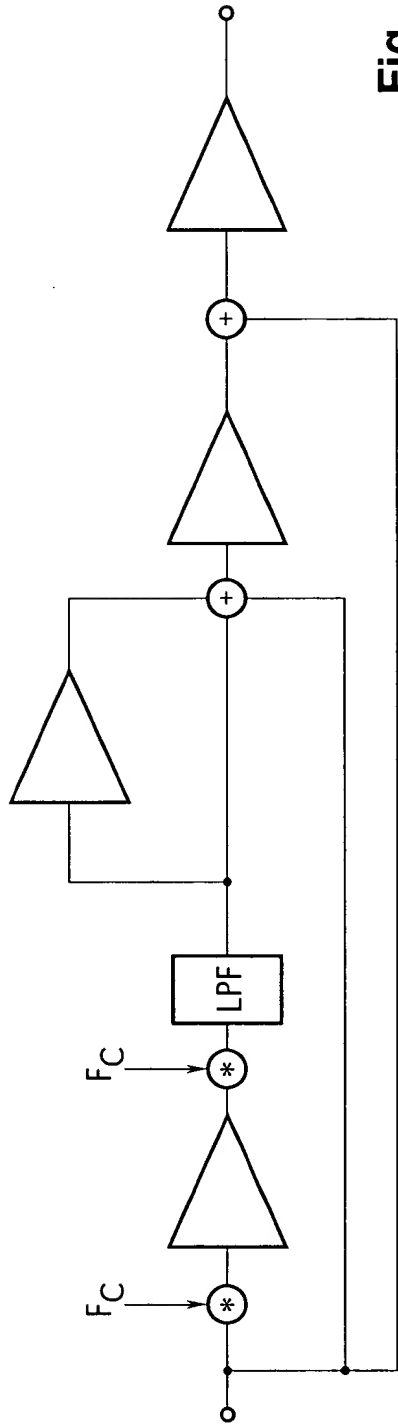


Fig. 1.3

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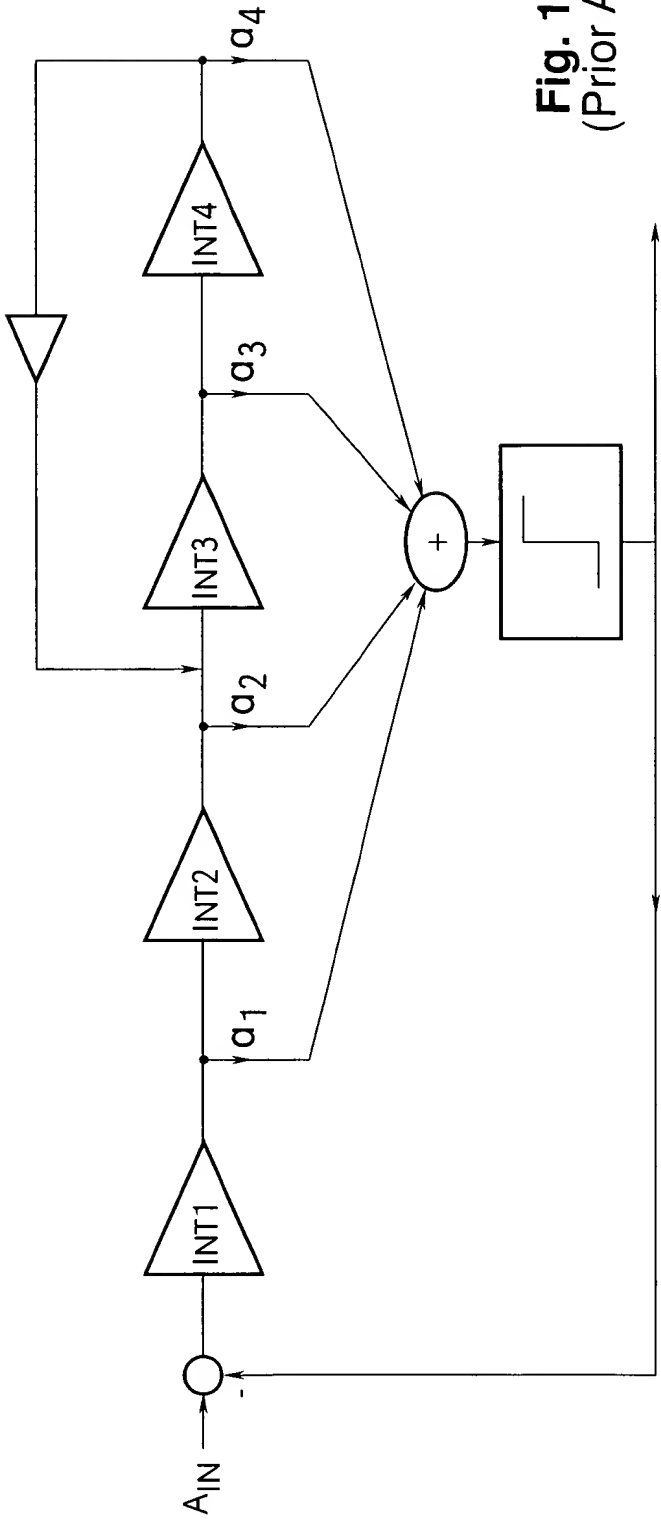


Fig. 1.4  
(Prior Art)

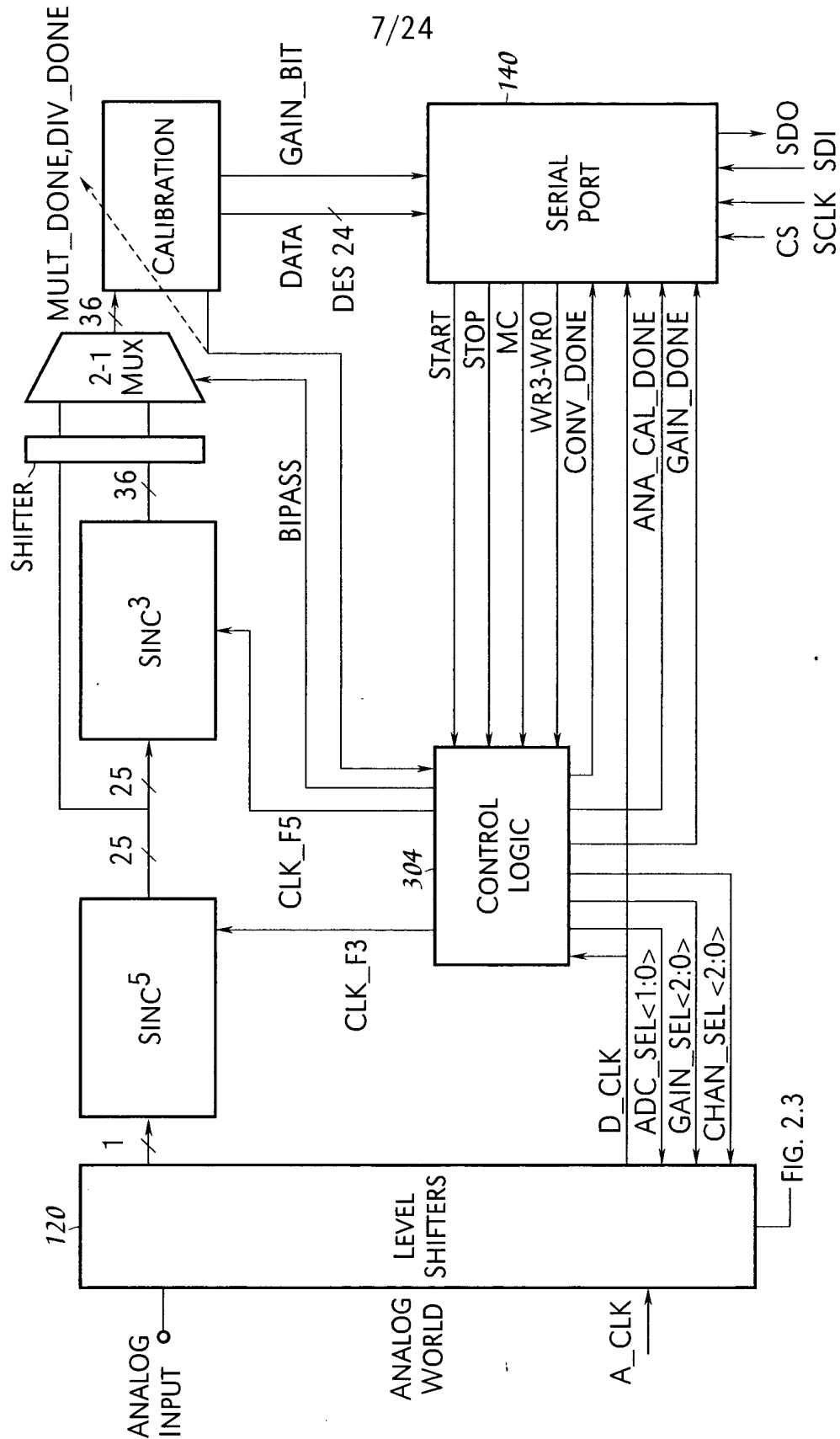


Fig. 1.5A



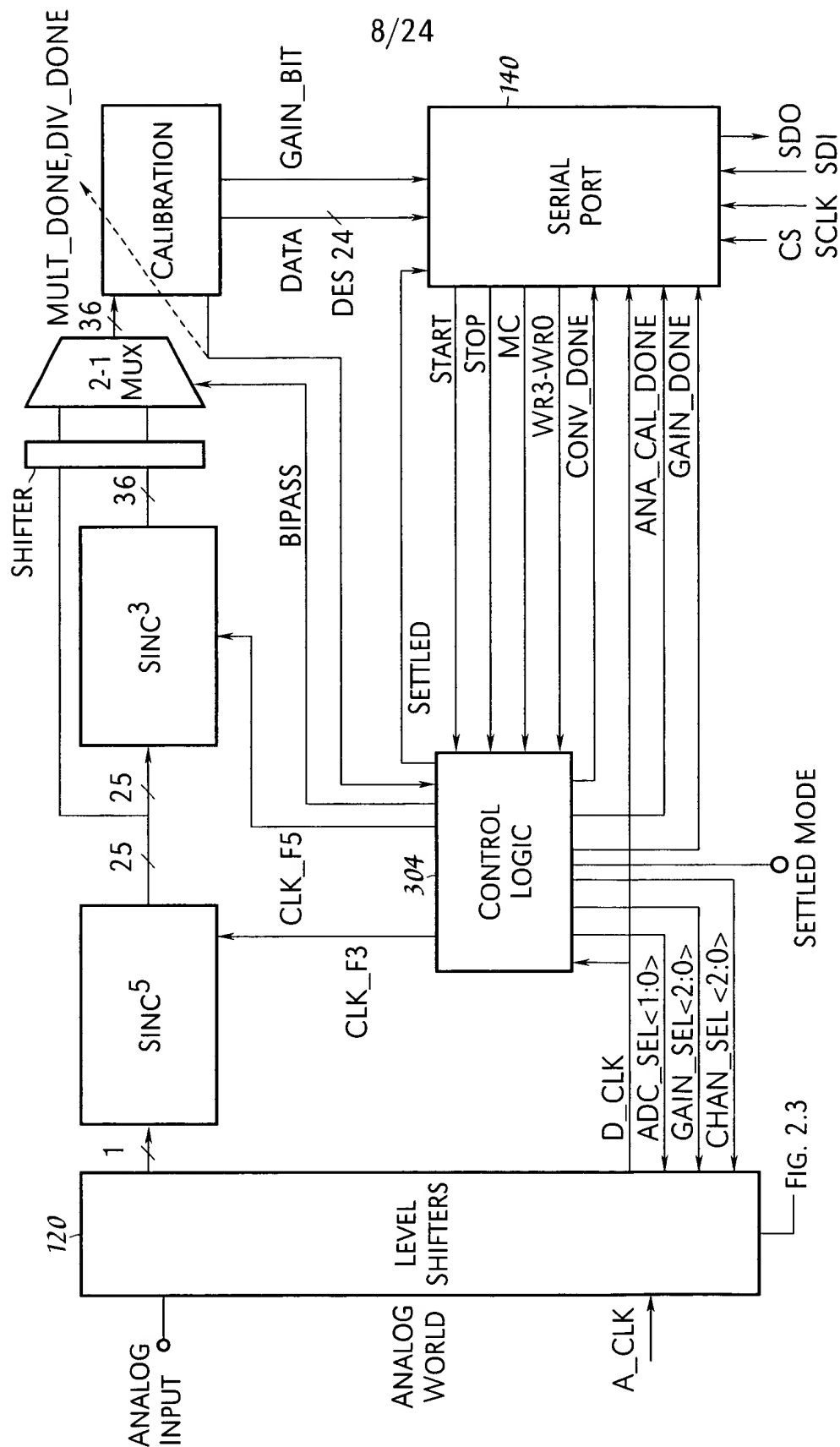


Fig. 1.5B

SETTLED MODE

FIG. 2.3



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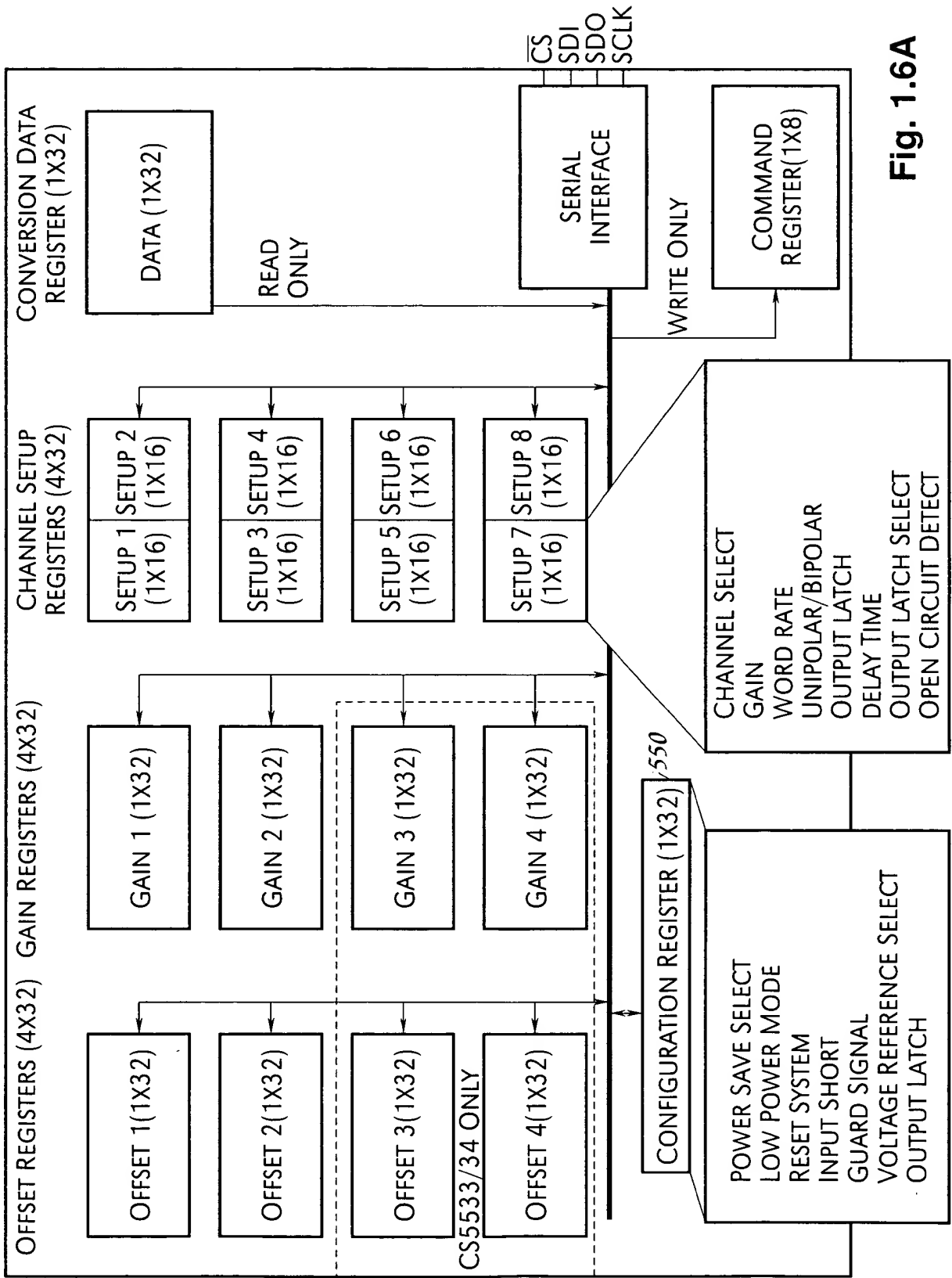


Fig. 1.6A

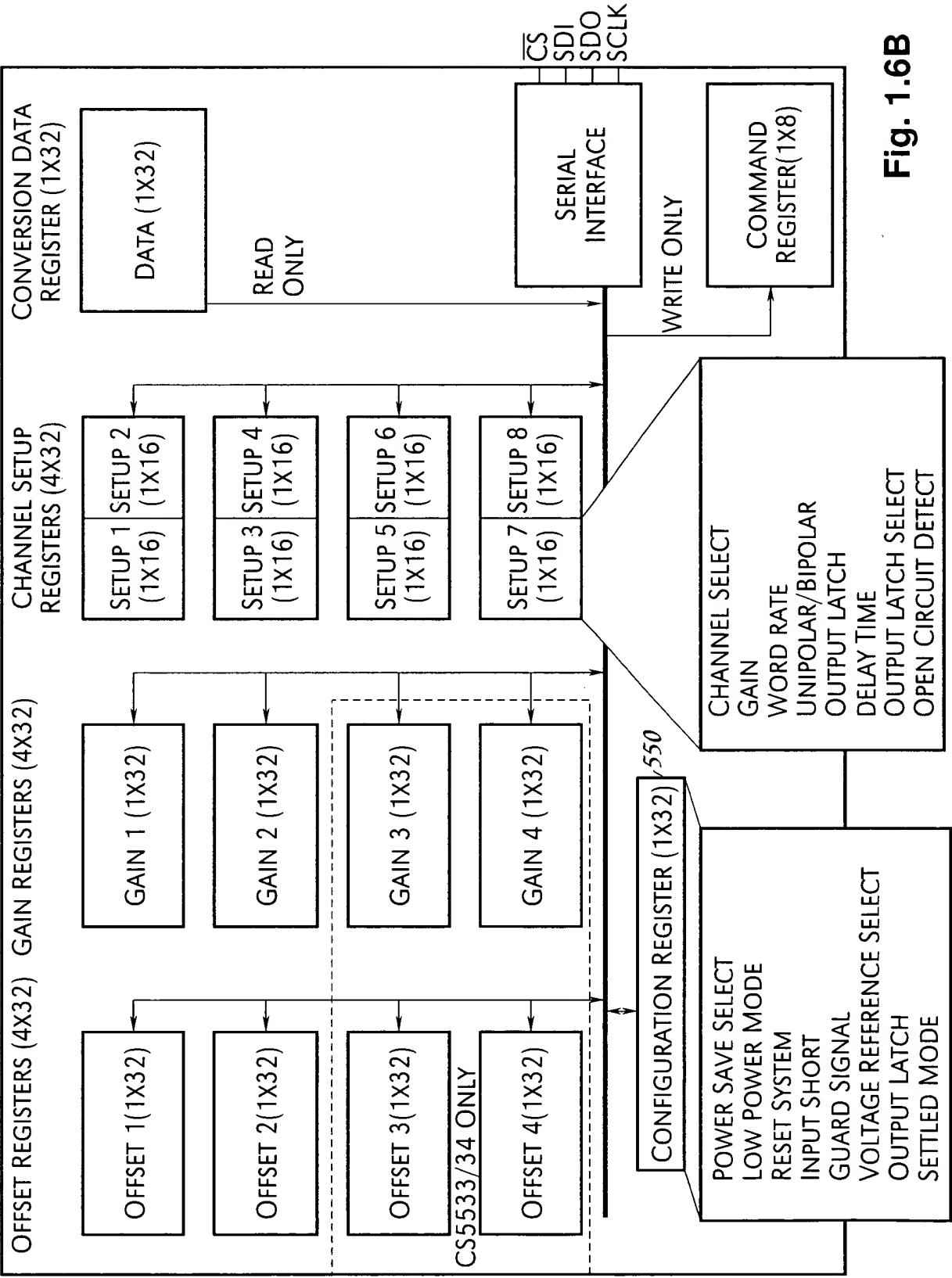


Fig. 1.6B



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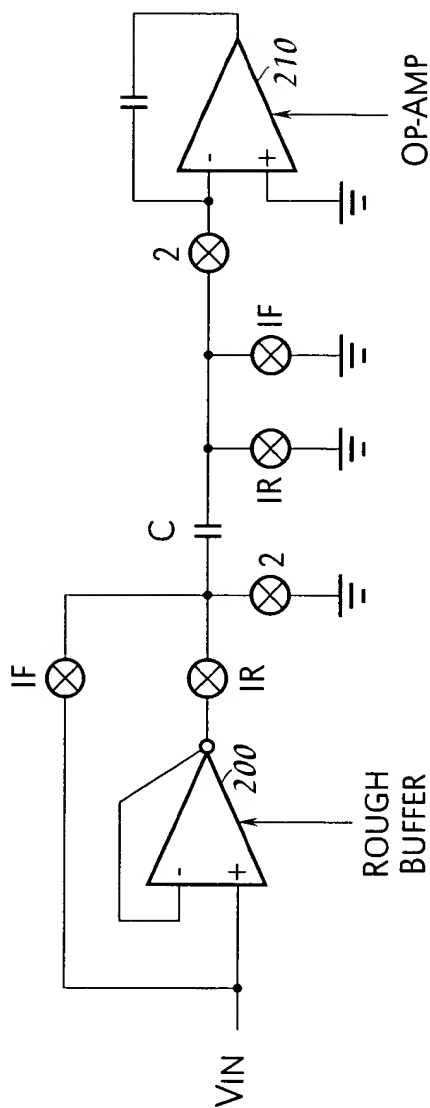


Fig. 2.0

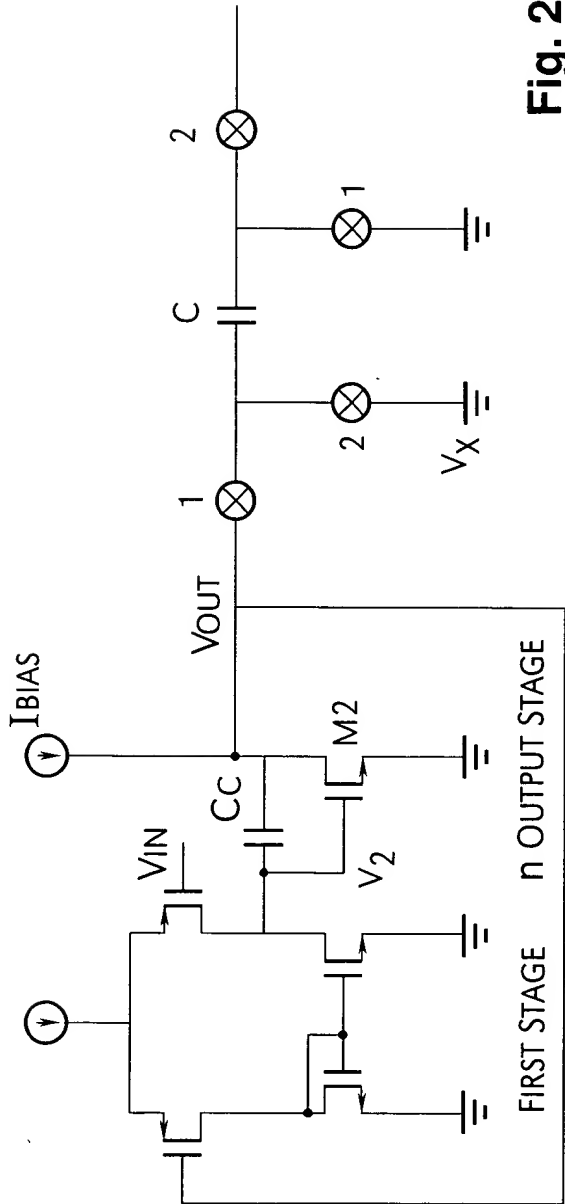


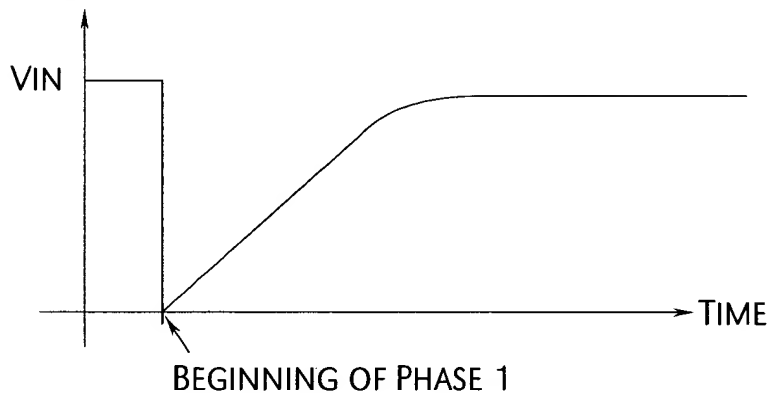
Fig. 2.1



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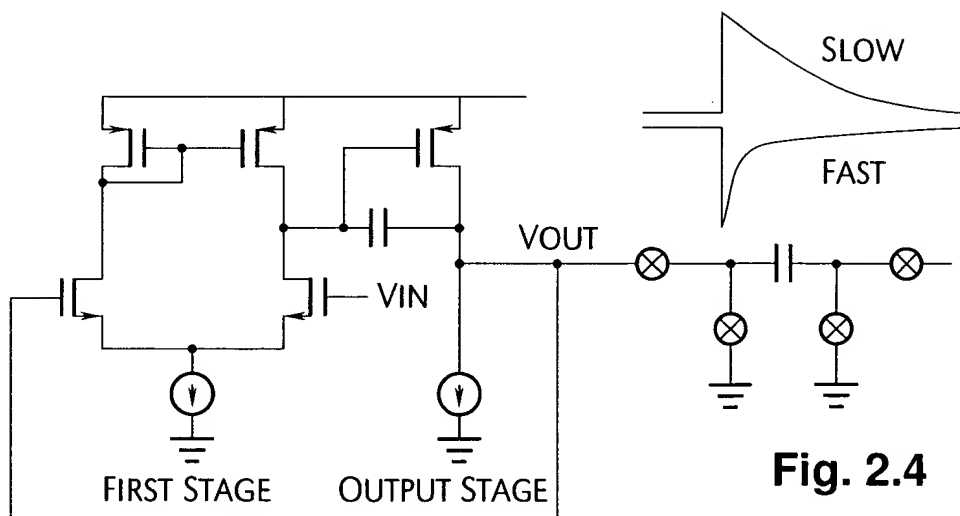
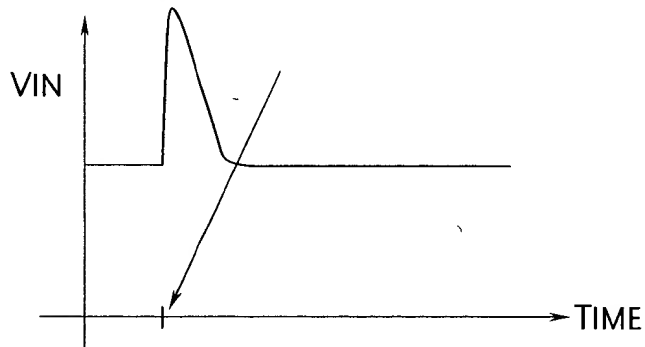
$V_{IN} = \text{CONSTANT}$   
 $V_{OUT} > V_X$

VOLTAGE  $V_{OUT}$



$V_{IN} = \text{CONSTANT}$   
 $V_{OUT} < V_X$

VOLTAGE  $V_{OUT}$



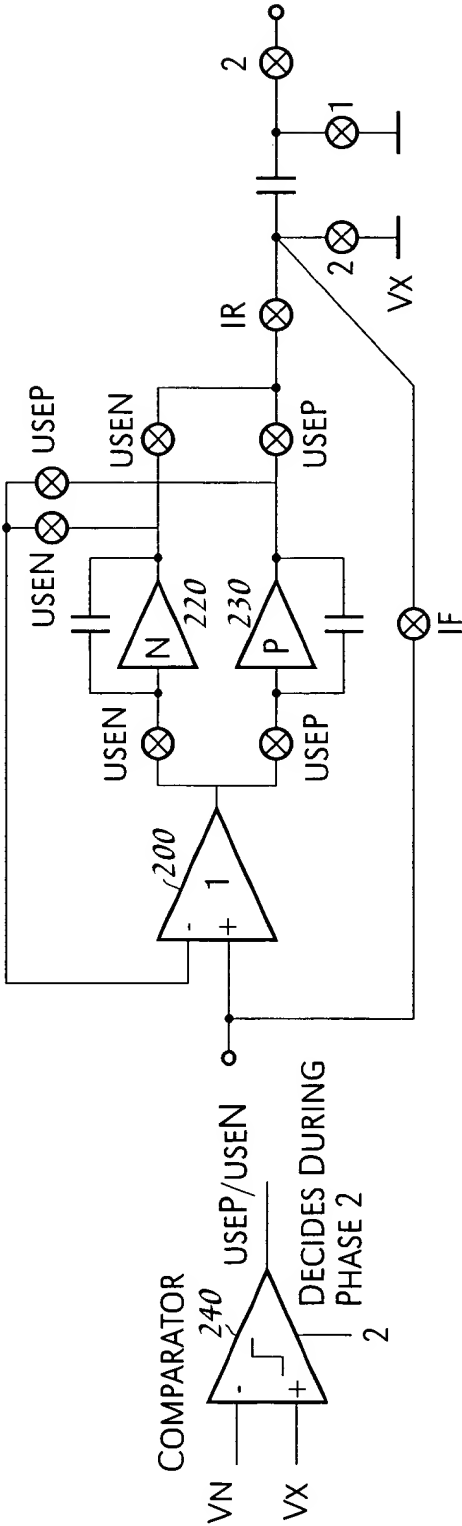


Fig. 2.5



Fig. 2.6

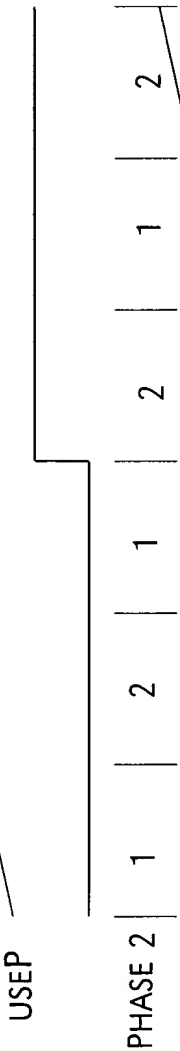


Fig. 2.7



Fig. 2.8

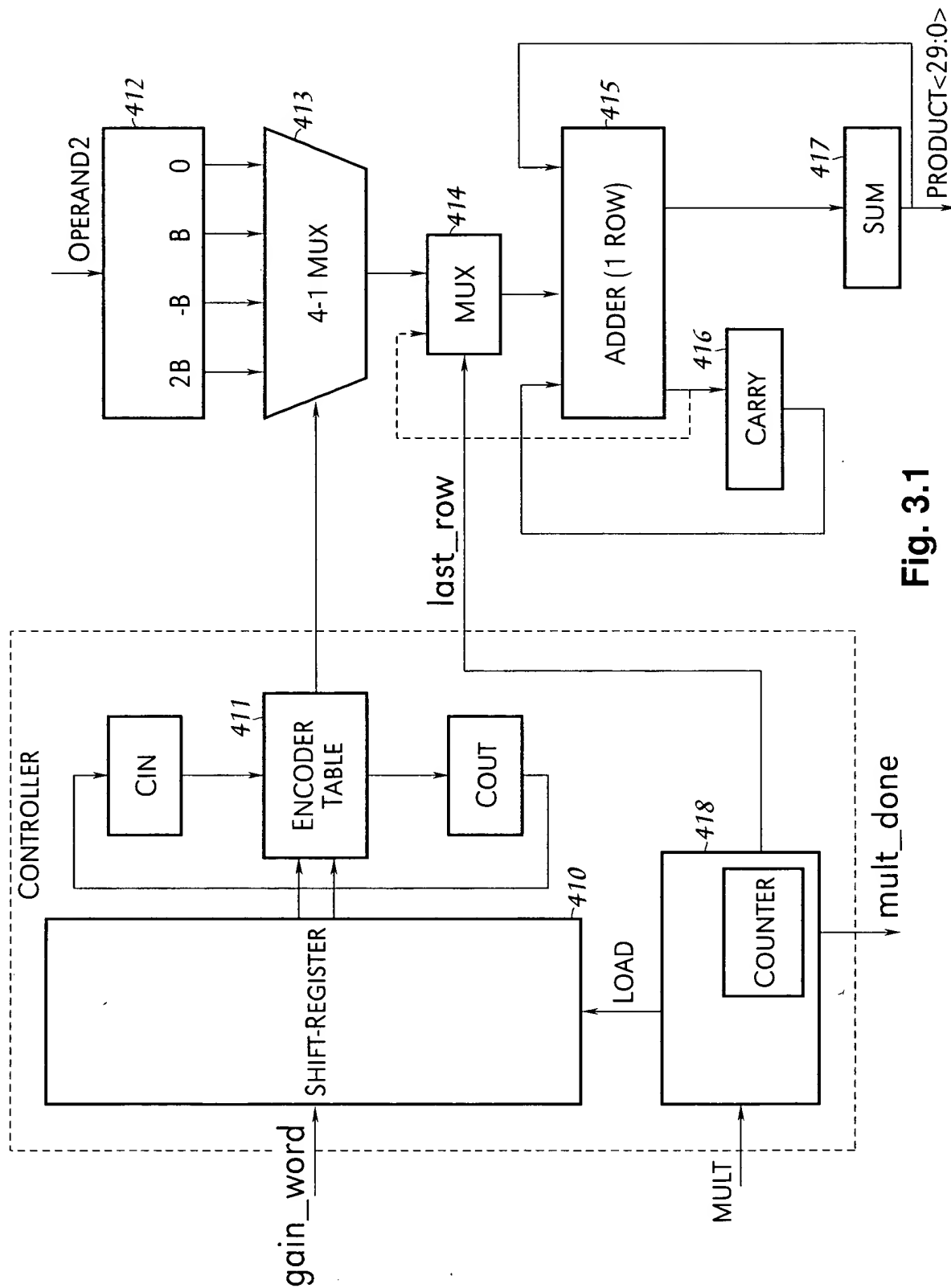


Fig. 3.1



TABLE 2: ENCODING SCHEME PROPOSED

$A_{i+1}$	$A_i$	Operation
0	0	$R_i = R_{i-1}/4$
0	1	$R_i = (R_{i-1} + B)/4$
1	0	$R_i = (R_{i-1} + 2B)/4$
1	1	$R_i = (R_{i-1} + 3B)/4$

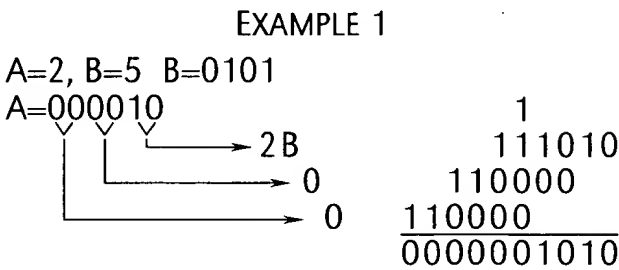
**Fig. 3.2**  
(PRIOR ART)

TABLE 3: CARRY PROPAGATE ENCODING SCHEME

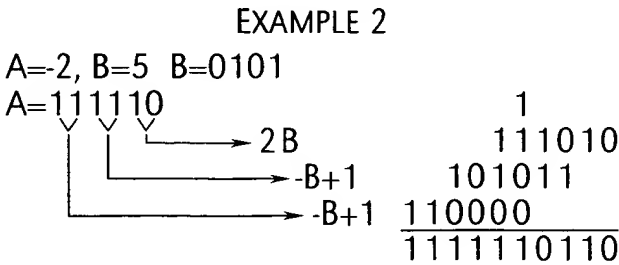
$C_{in}$	$A_{i+1}$	$A_i$	Operation	$C_{out}$
0	0	0	$R_i = R_{i-1}/4$	0
0	0	1	$R_i = (R_{i-1} + B)/4$	0
0	1	0	$R_i = (R_{i-1} + 2B)/4$	0
0	1	1	$R_i = (R_{i-1} - B)/4$	1
1	0	0	$R_i = (R_{i-1} + B)/4$	0
1	0	1	$R_i = (R_{i-1} + 2B)/4$	0
1	1	0	$R_i = (R_{i-1} - B)/4$	0
1	1	1	$R_i = (R_{i-1})/4$	1

**Fig. 3.3**  
(PRIOR ART)

**Fig. 3.4**



**Fig. 3.5**





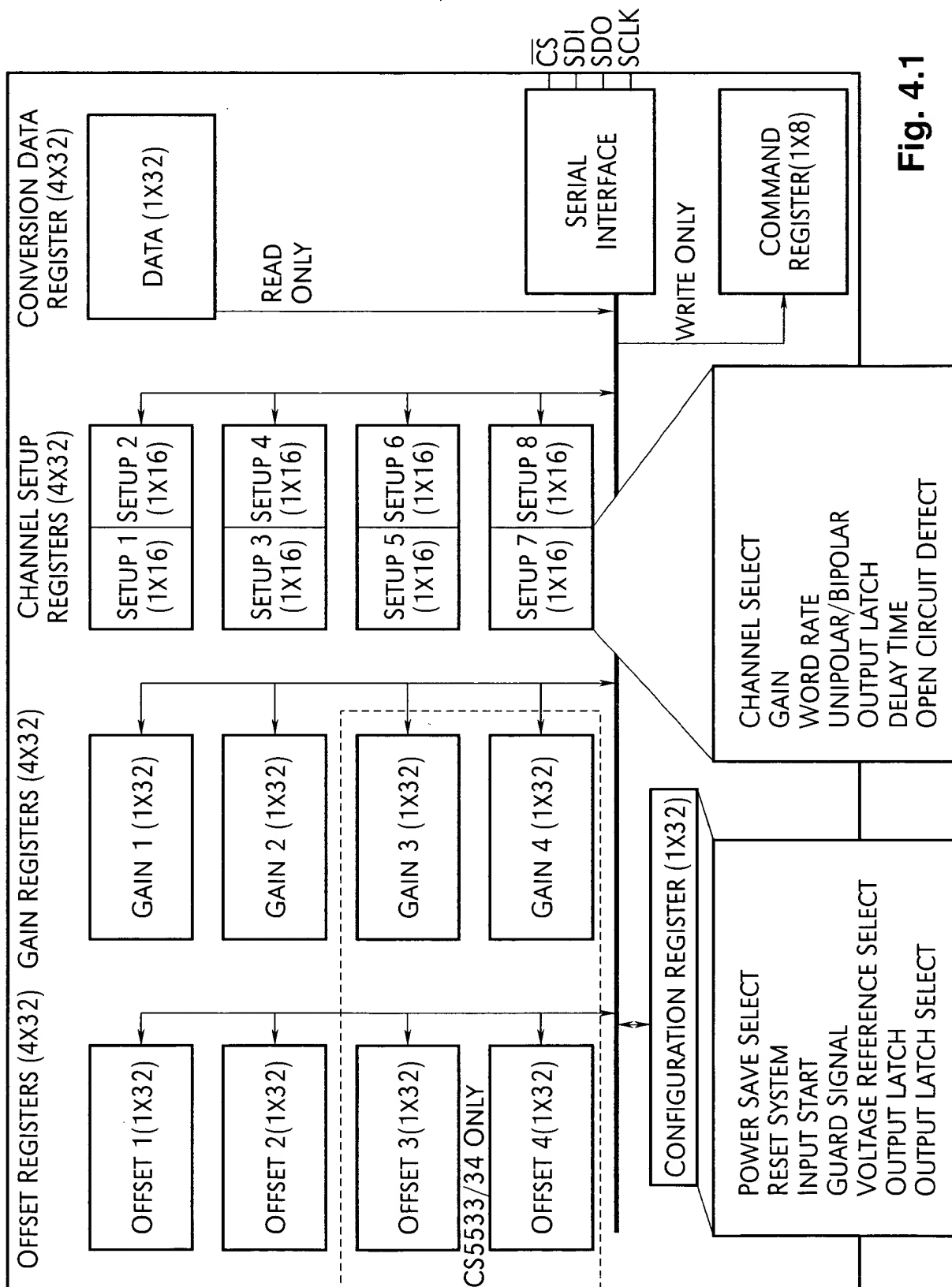


Fig. 4.1



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D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	ARA	CS1	CS0	R/W	RSB2	RSB1	RSB0

BIT	NAME	VALUE	FUNCTION
D7	COMMAND BIT, C	0 1	MUST BE LOGIC 0 FOR THESE COMMANDS. THESE COMMANDS ARE INVALID IF THIS BIT IS LOGIC 1.
D6	ACCESS REGISTERS AS ARRAYS, ARA	0 1	IGNORE THIS FUNCTION. ACCESS THE RESPECTIVE REGISTERS, OFFSET, GAIN, OR CHANNEL-SETUP, AS AN ARRAY OF REGISTERS. THE PARTICULAR REGISTERS ACCESSED ARE DETERMINED BY THE RS BITS. THE REGISTERS ARE ACCESSED MSB FIRST WITH PHYSICAL CHANNEL 0 ACCESSED FIRST FOLLOWED BY PHYSICAL CHANNEL 1 NEXT AND SO FORTH.
D5-D4	CHANNEL SELECT BITS, CS1-CS0	00 01 10 11	CS1-CS0 PROVIDE THE ADDRESS OF ONE OF THE TWO (FOUR FOR CS5533/34) PHYSICAL INPUT CHANNELS. THESE BITS ARE ALSO USED TO ACCESS THE CALIBRATION REGISTERS ASSOCIATED WITH THE RESPECTIVE PHYSICAL INPUT CHANNEL. NOTE THAT THESE BITS ARE IGNORED WHEN READING DATA REGISTER.
D3	READ/WRITE, R/W	0 1	WRITE TO SELECTED REGISTER. READ FROM SELECTED REGISTER.
D2-D0	REGISTER SELECT BIT, RSB3-RSB0	000 001 010 011 100 101 110 111	RESERVED OFFSET REGISTER GAIN REGISTER CONFIGURATION REGISTER CONVERSION DATA REGISTER (READ ONLY) CHANNEL-SETUP REGISTERS RESERVED RESERVED

**Fig. 4.2**



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D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

BIT NAME VALUE FUNCTION

D7 COMMAND BIT, C 0 THESE COMMANDS ARE INVALID IF THIS BIT IS LOGIC 0.  
1 MUST BE LOGIC 1 FOR THESE COMMANDS.

D6 MULTIPLE CONVERSIONS, MC 0 PERFORM FULLY SETTLED SINGLE CONVERSIONS.  
1 PERFORM CONVERSIONS CONTINUOUSLY.

D5-D3 CHANNEL-SETUP REGISTER POINTER BITS, CSRP 000 THESE BITS ARE USED AS POINTERS TO THE CHANNEL-SETUP REGISTERS. EITHER A SINGLE CONVERSION OR CONTINUOUS CONVERSIONS ARE PERFORMED ON THE CHANNEL SETUP REGISTER POINTED TO BY THESE BITS.  
...  
111

D2-D0 CONVERSION/CALIBRATION BITS, CC2-CC0 000 NORMAL CONVERSION  
001 SELF-OFFSET CALIBRATION  
010 SELF-GAIN CALIBRATION  
011 RESERVED  
100 RESERVED  
101 SYSTEM-OFFSET CALIBRATION  
110 SYSTEM-GAIN CALIBRATION  
111 RESERVED

Fig. 4.3



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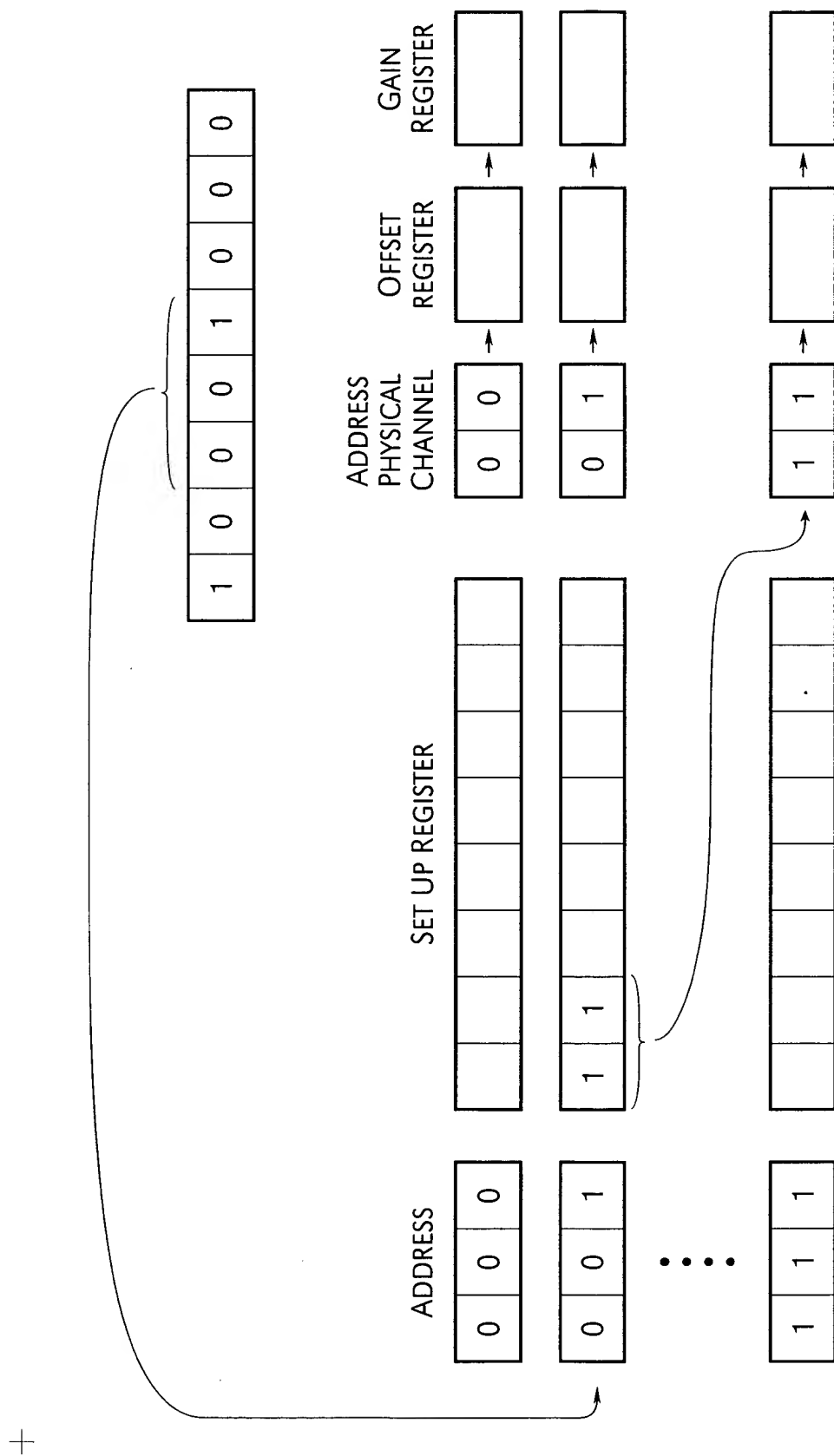


Fig. 4.4

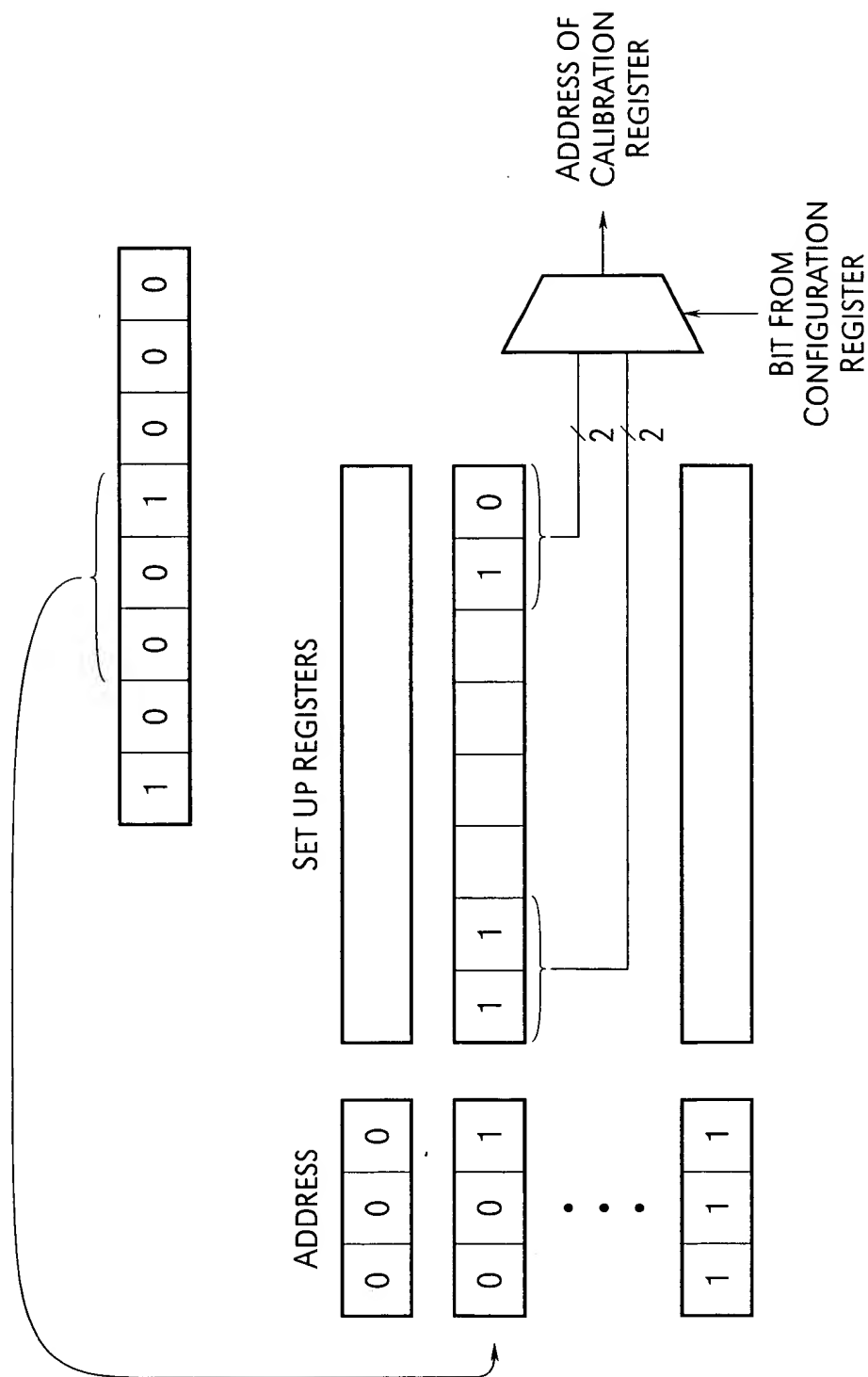


Fig. 4.5

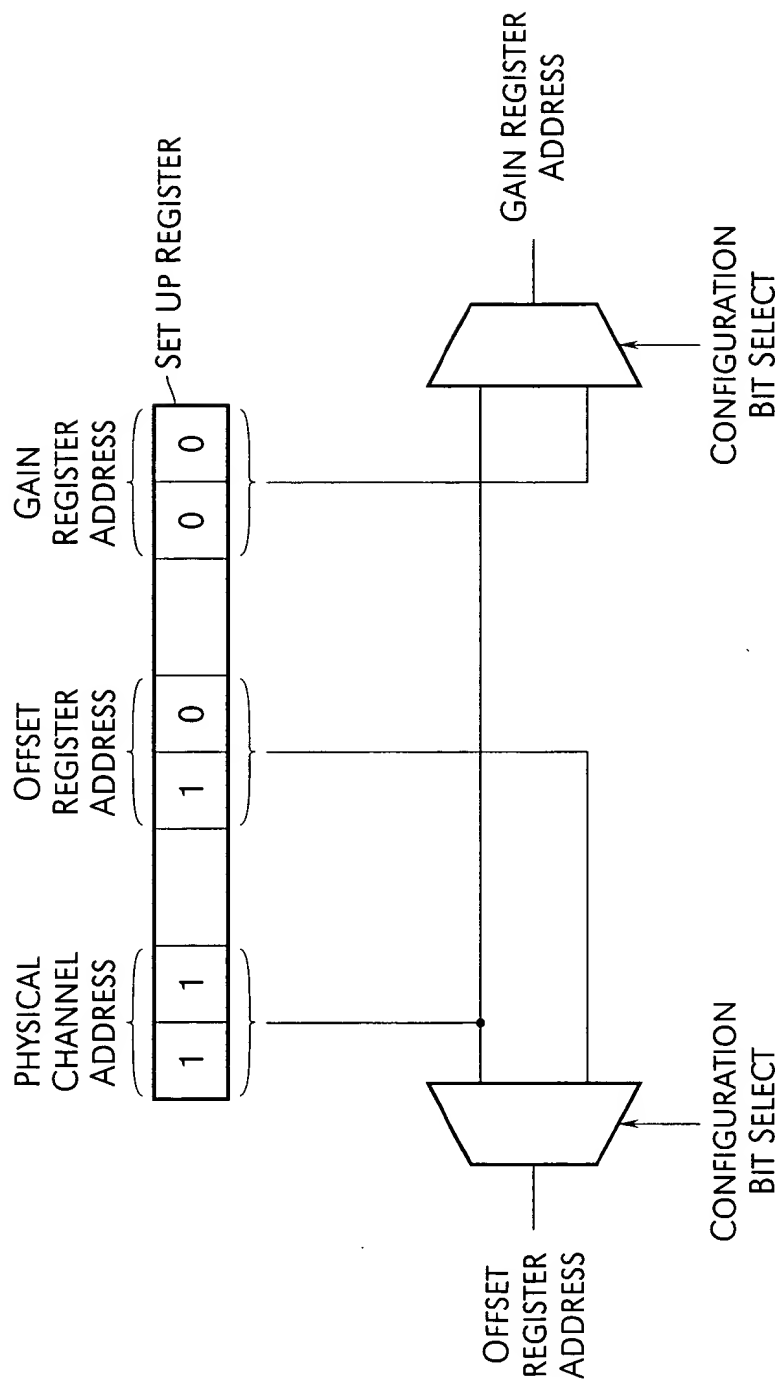
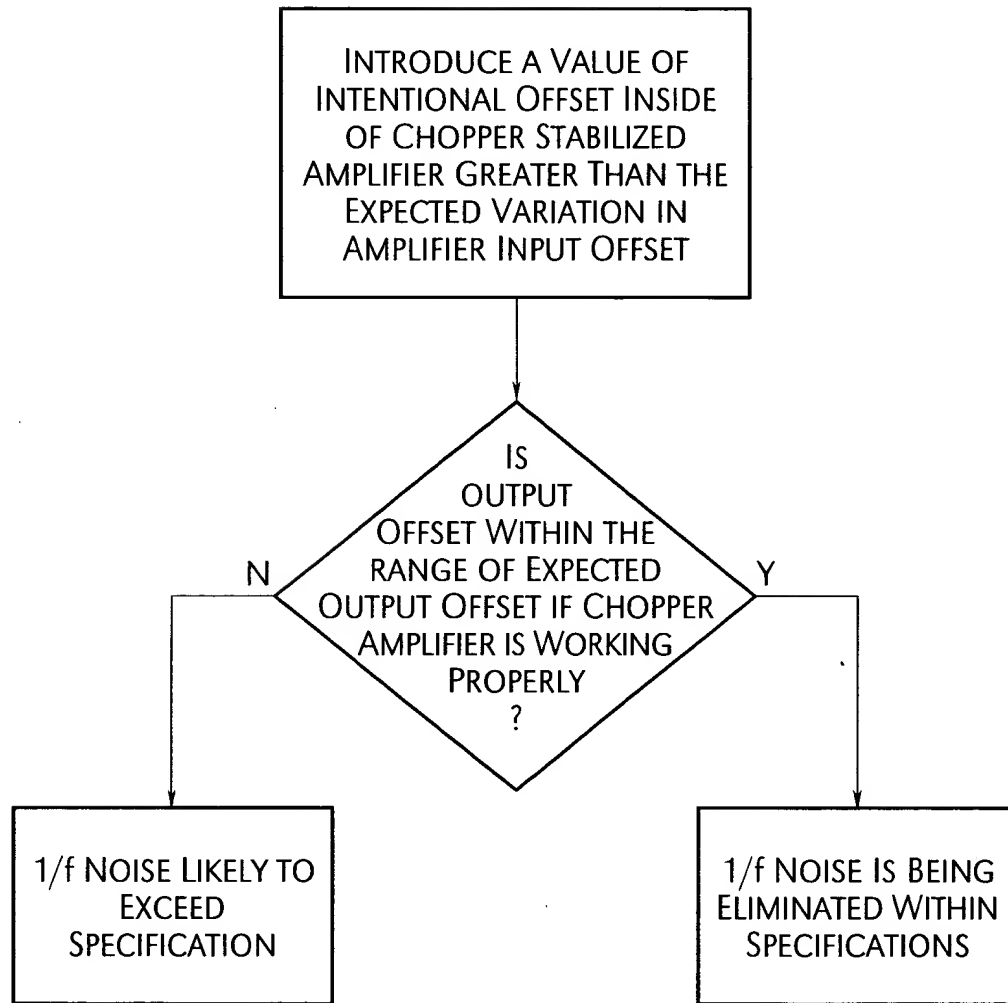
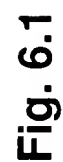


Fig. 4.6



**Fig. 5.1**





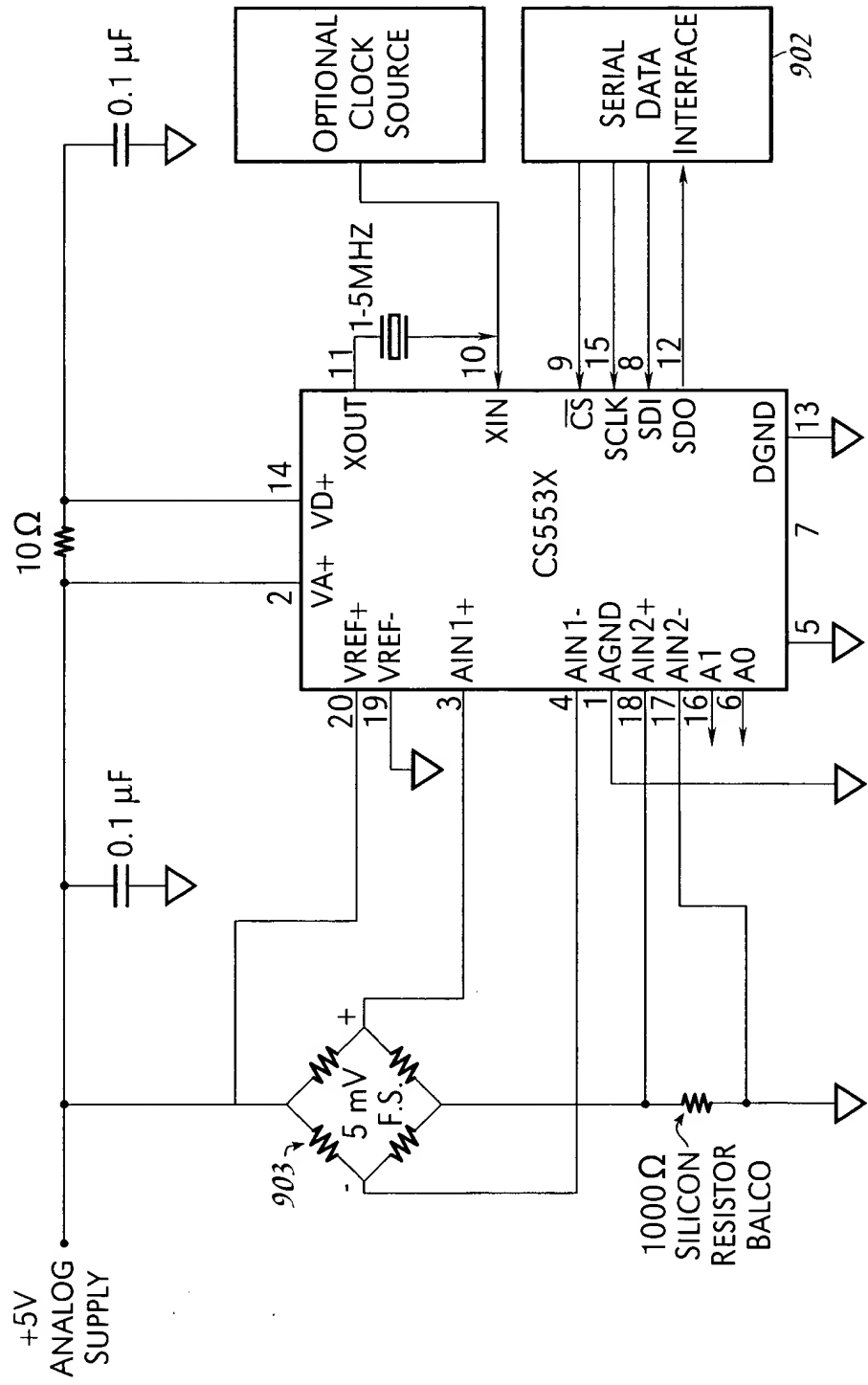


Fig. 6.2